

COMPAL CONFIDENTIAL

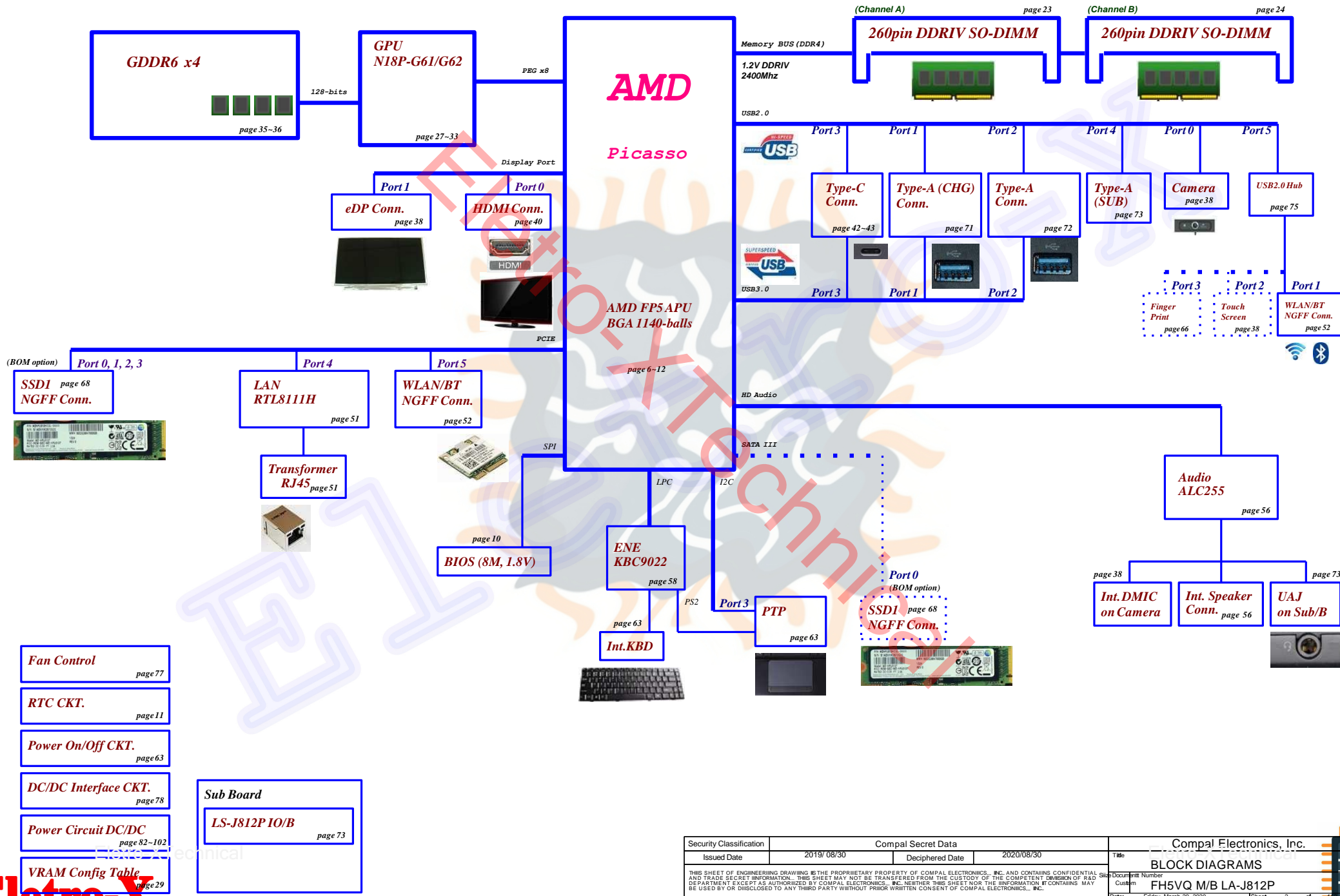
FH5VQ MB Schematics Document

AMD Picasso Platform
nVidia N18P-G61/G62

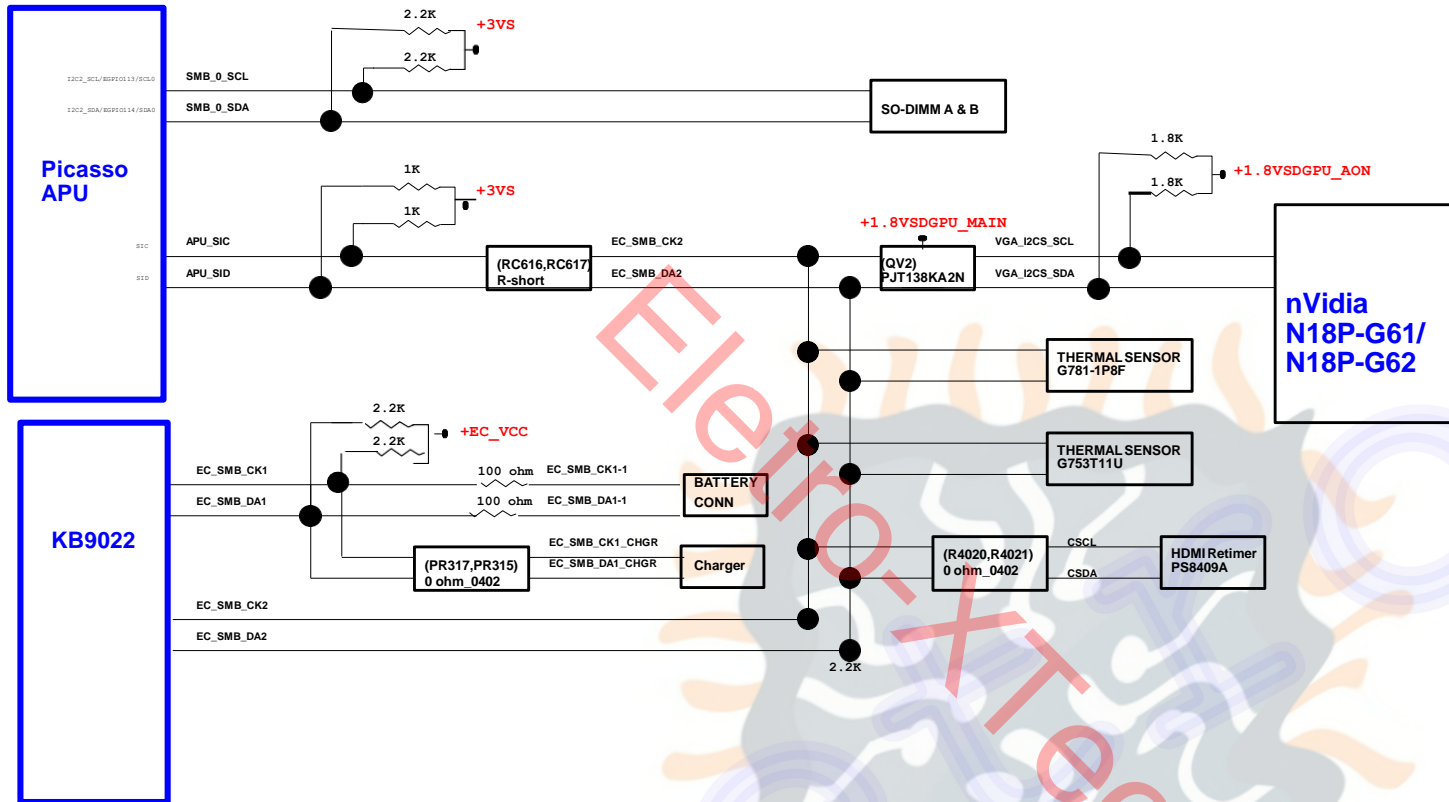
LA-J812P REV:1A
2020-03-09

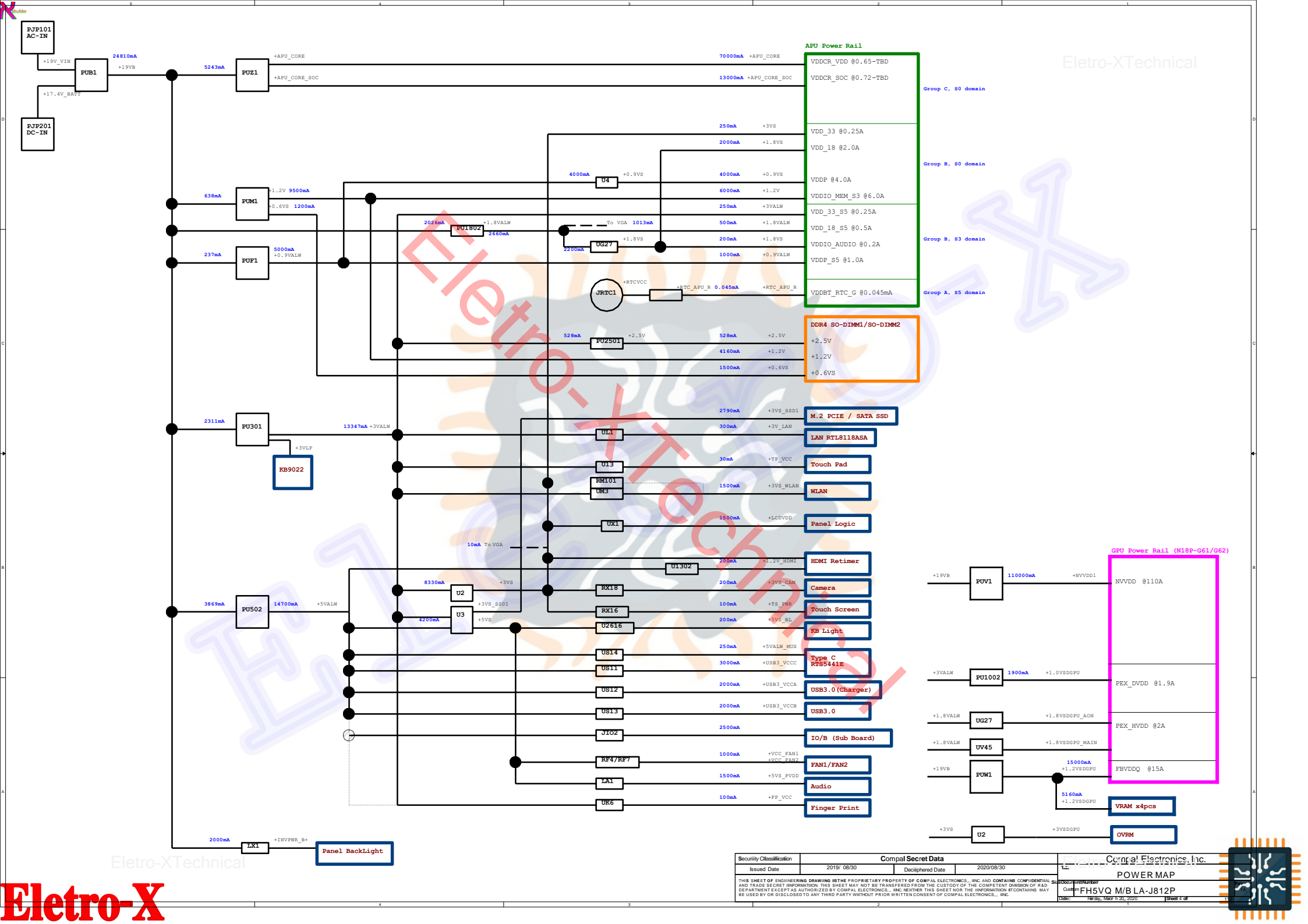
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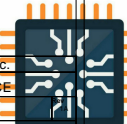
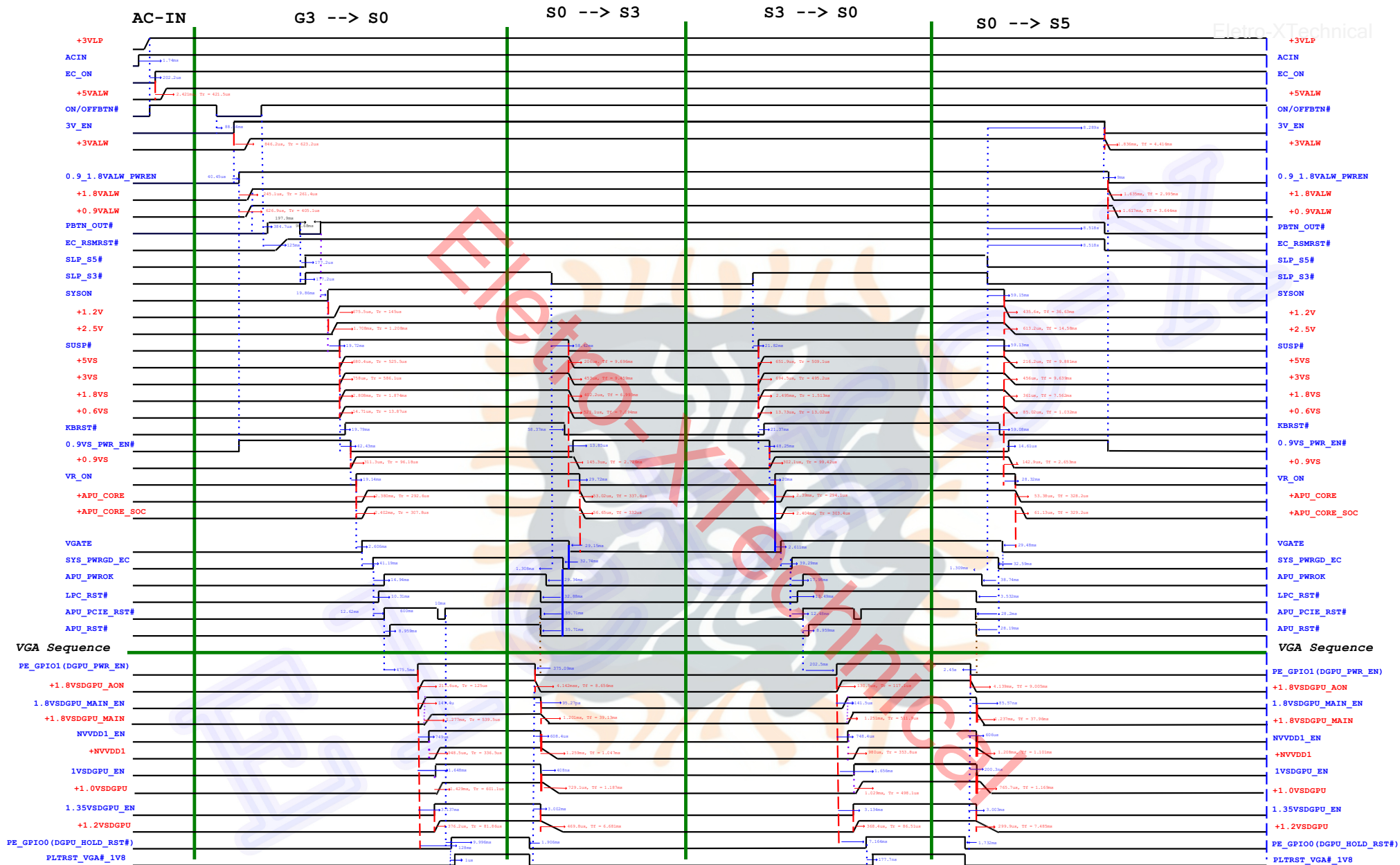


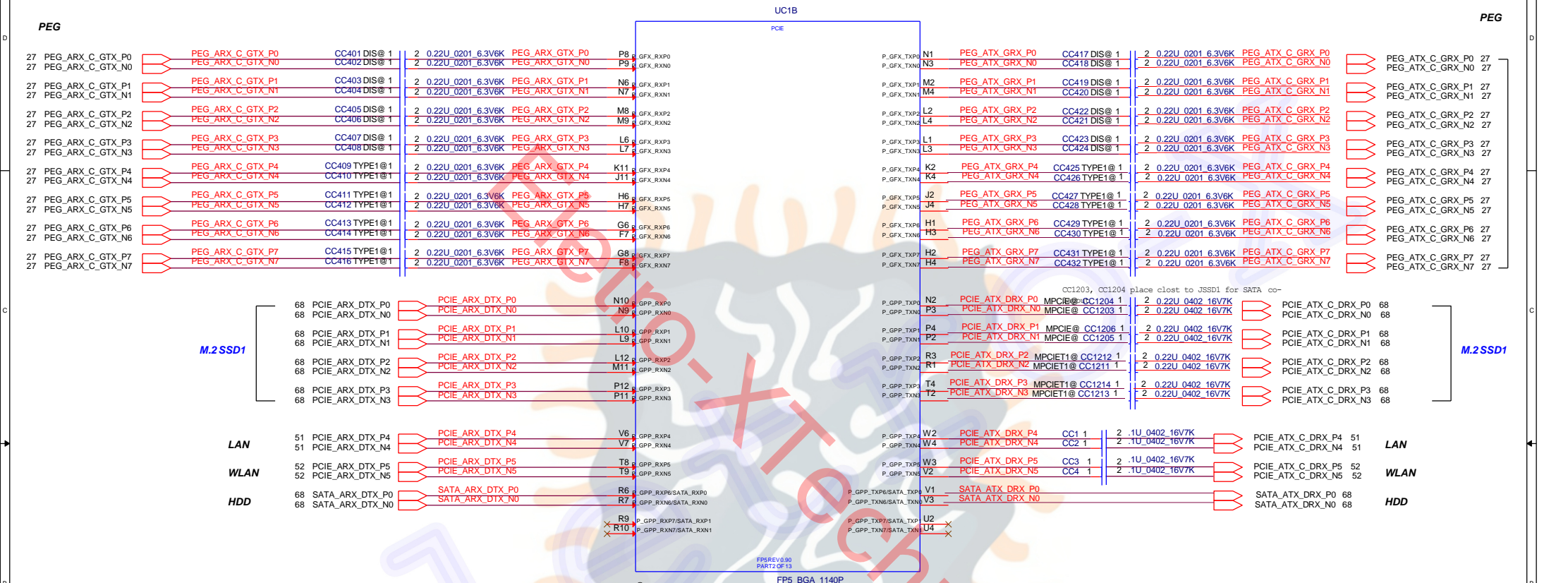


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				Customer
				Date
				Sheet
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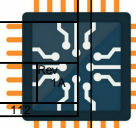

APU PN Table

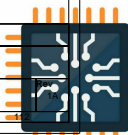
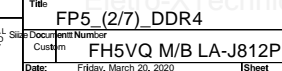
APU Platform	Customer PN	Customer PN	Customer PN	Customer PN	Compal PN	Compal PN
Picasso		UC1 R5APU@	UC1 R7APU@			
						
		S I C RYZEN5 YM3500C4T4MFG 2.1G APU ABO!	S I C RYZEN7 YM3700C4T4MFG 2.3G APU ABO!			
		SA0000CCR60	SA0000C7680			

PCB Number

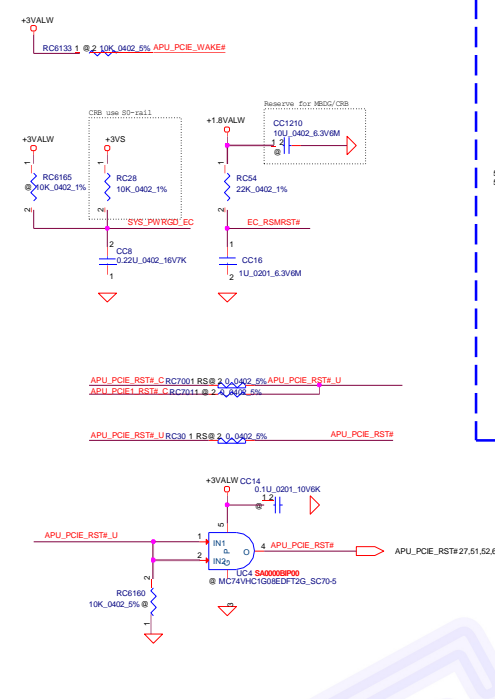
ZZZ EVT@ PCB 2Y2 LA-J812P REV0 MB 1 DAA000N4000	ZZZ PVT@ PCB FH5VQ LA-J812PLS-J812P DAZZY200101 MB: DAA000N401A Rev1A IO/B: DAA000N5010 Rev1.0
ZZZ DVT@ PCB FH5VQ LA-J812PLS-J812P DAZZY200100 MB: DAA000N4010 Rev1.0 IO/B: DAA000N5010 Rev1.0	ZZZ MP@ PCB FH5VQ LA-J312PLS-J812P iJA22N2C101 MB: DAA000N401A Rev1A IO/B: DAA000N5010 Rev1.0

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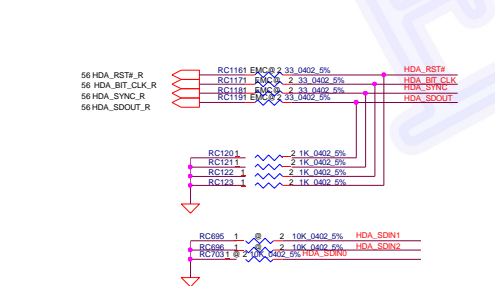




ACPI

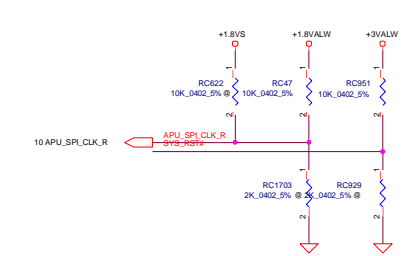


HDA



Strap Pin

	APU_SPI_CLK_R	SYS_RST#
H	USE 40MHz CRYSTAL CLOCK (Default)	NORMAL RESET MODE (Default)
L	USE 100MHz PCIE REFERENCE CLOCK	SHORT RESET MODE

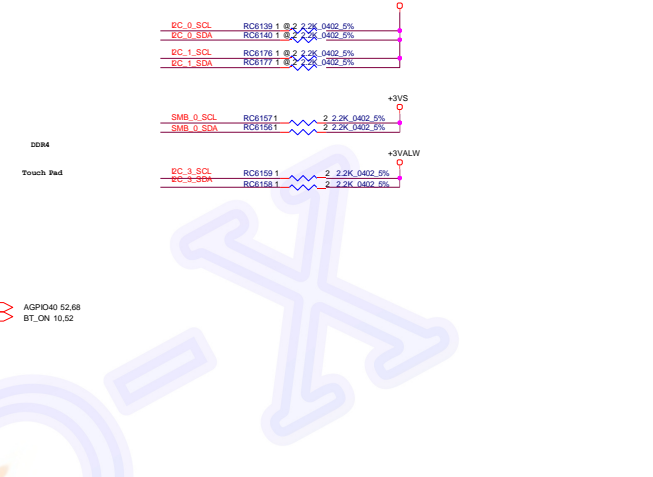
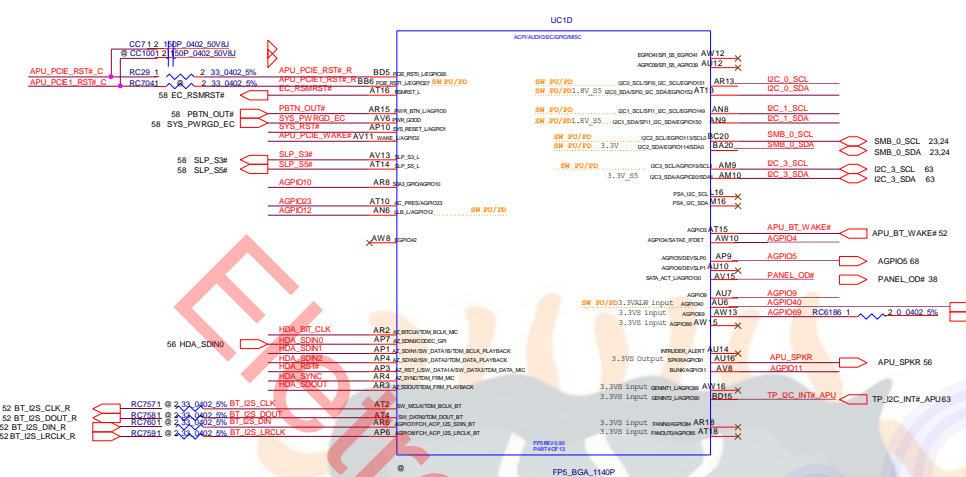
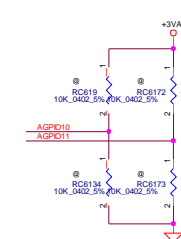
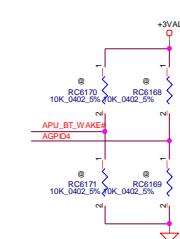
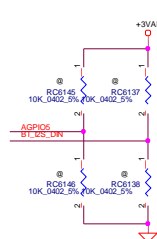


GPIO Table

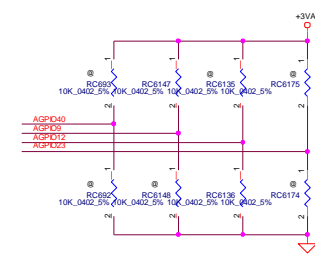
AGPIO5	AGPIO7 (BT_I2S_DIN)

AGPIO3	AGPIO4

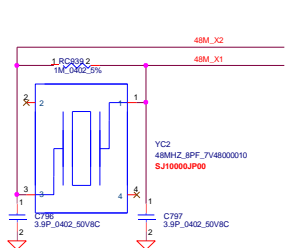
AGPIO10	AGPIO11



	AGPIO40	AGPIO9	AGPIO12	AGPIO23
H	RSV	Type1	RSV	RSV
L	RSV	RSV	DMIC x2	RSV

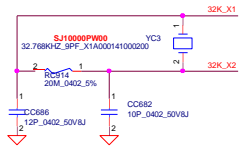


48MHz CRYSTAL

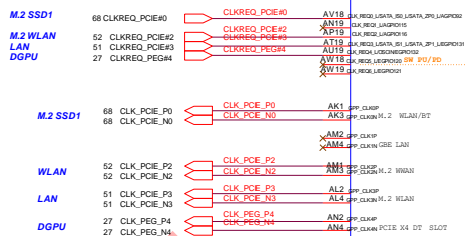


32.768KHz CRYSTAL

(55597) FFS 32.768K ± 20ppm 8331 <63K uha)

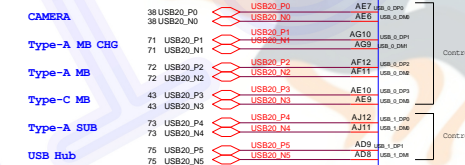


USB Function



52 SUSCLK_WLAN

RC782.1 @ 2.25, 0.402, 5% RTCCLOCK



APU_USBC_SCL

APU_USBC_SDA

RC8167

9.52 BT_ON

52 APU_WLAN_WAKEUP

APU_WLAN_WAKEUP

APU_WLAN_WAKEUP

APU_WLAN_WAKEUP

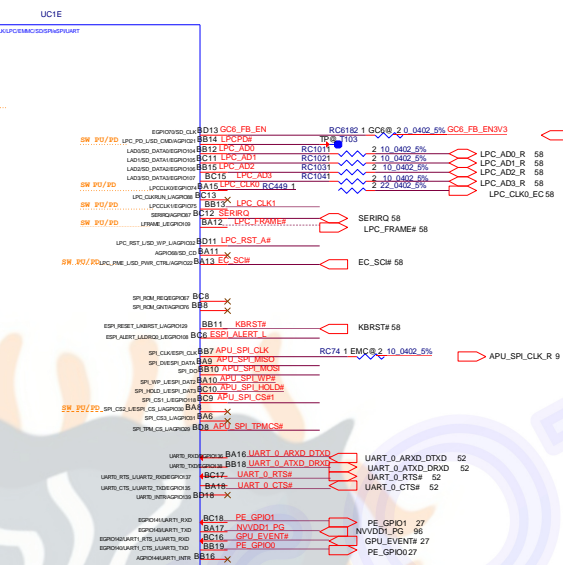
APU_WLAN_WAKEUP

APU_WLAN_WAKEUP

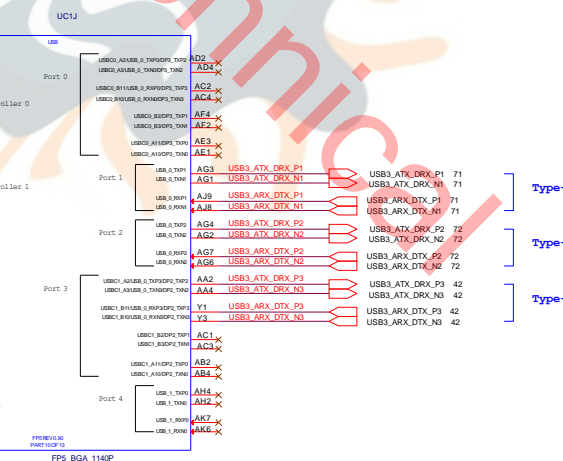
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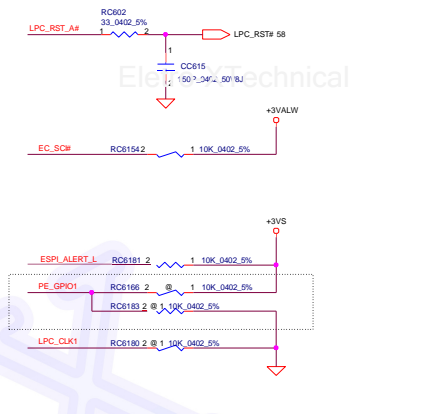
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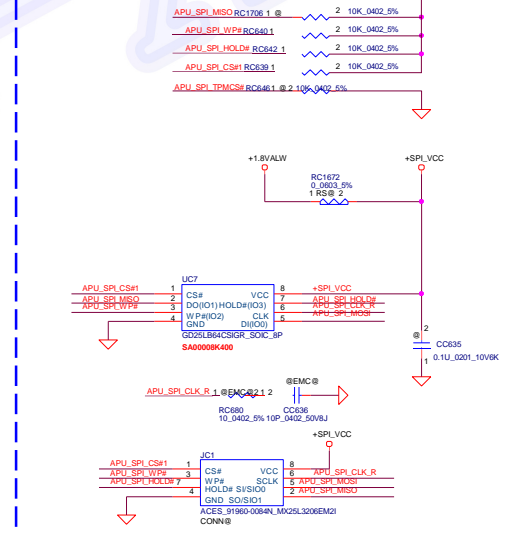
FPS_BGA_1140P



FPS_BGA_1140P



8MB SPI ROM

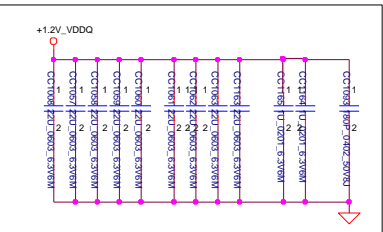


Type-A MB CHG

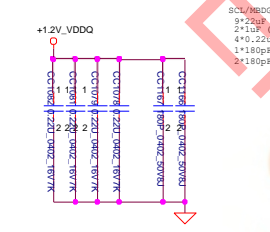
Type-A MB

Type-C MB

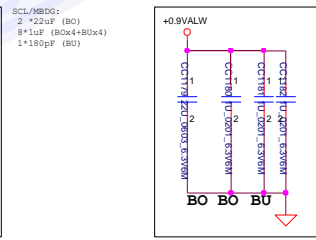
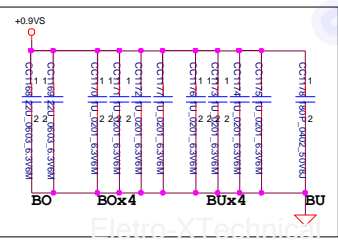
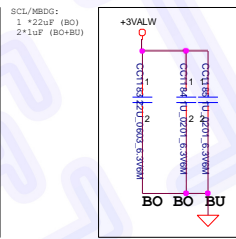
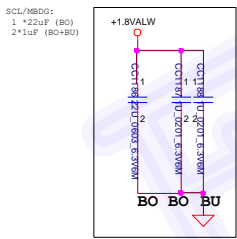
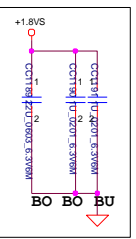
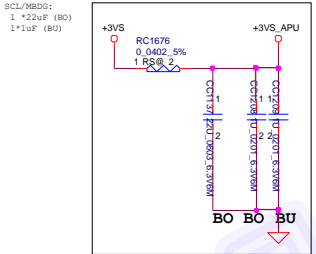
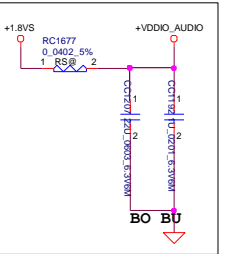
+APU_CORE SOC Cap
place at Power Side



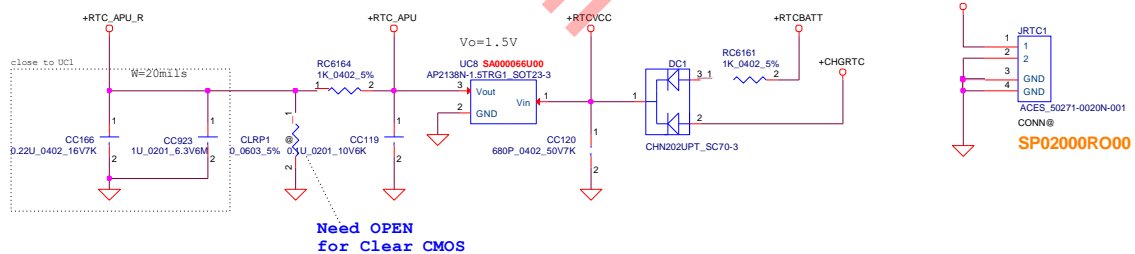
All BU(on bottom side under SOC)



ACROSS VDDIO AND VSS SPLIT

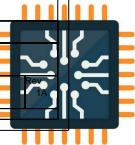


RTC OF APU



Need OPEN
for Clear CMOS

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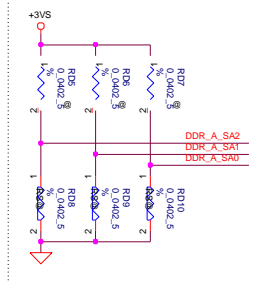
Eletro-X



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2-3A to 1 DIMMs/channel

Address : A0

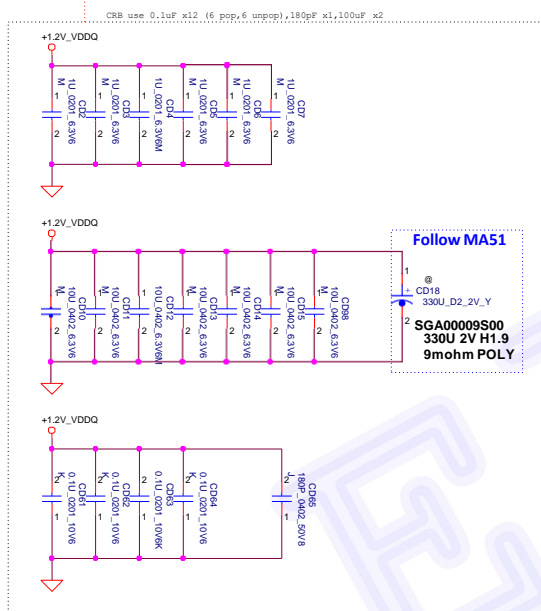


Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF DO at the DIMM socket

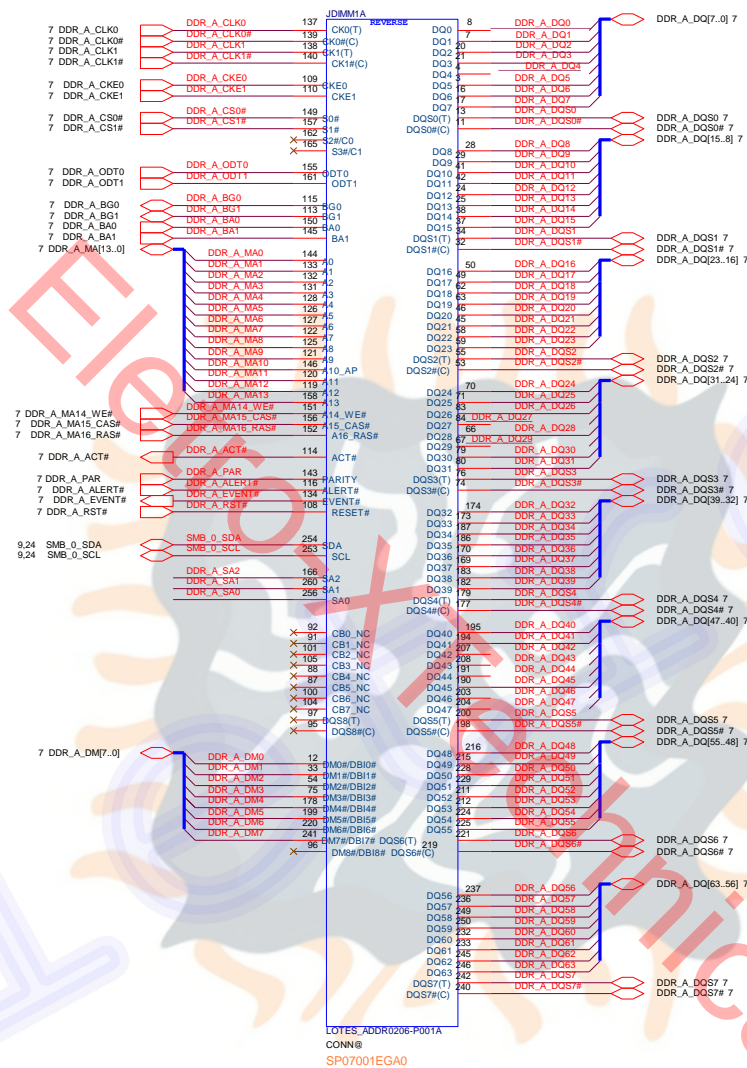
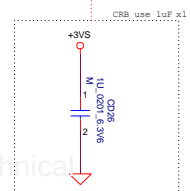
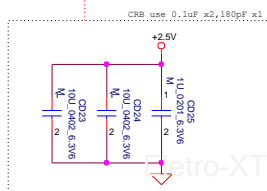


DDR4 support Even Parity check in DRAMs

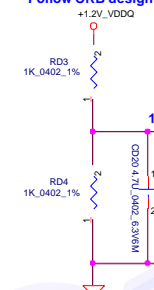


Layout Note:
Place near JDIMM1.257.259

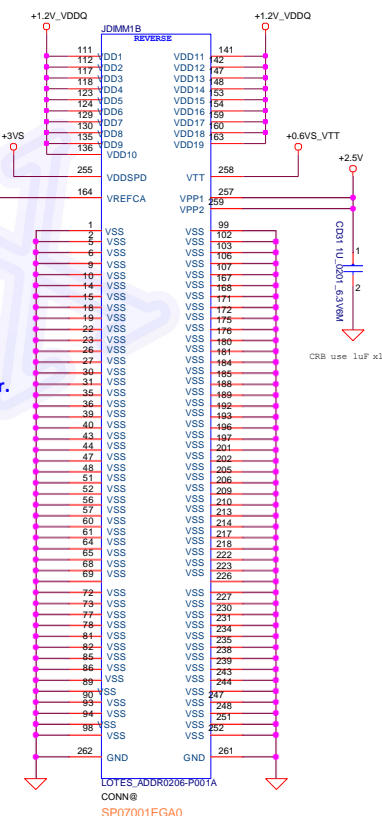
Layout Note:
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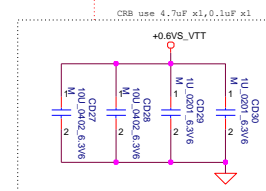
Follow CRB design



Place near to SO-DIMM connector.

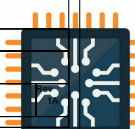


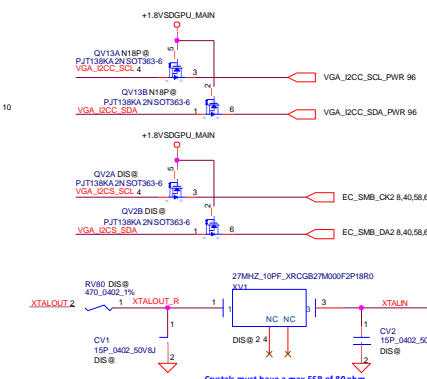
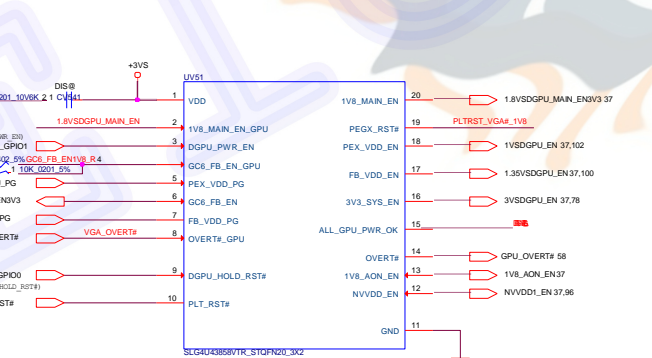
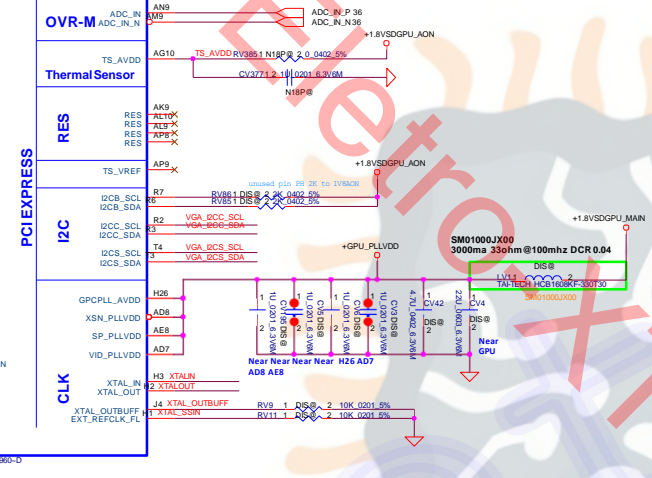
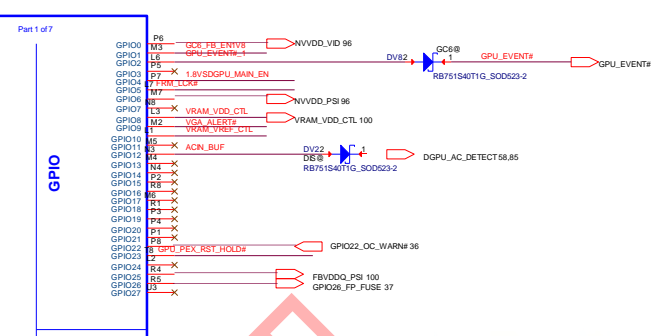
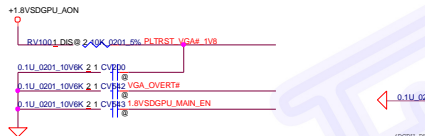
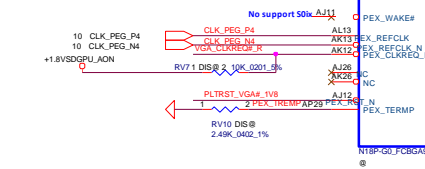
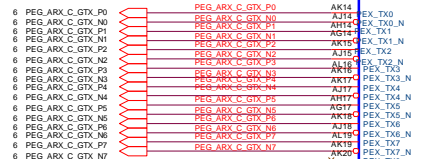
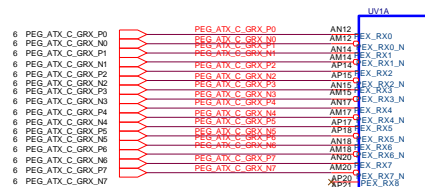
Layout Note:
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




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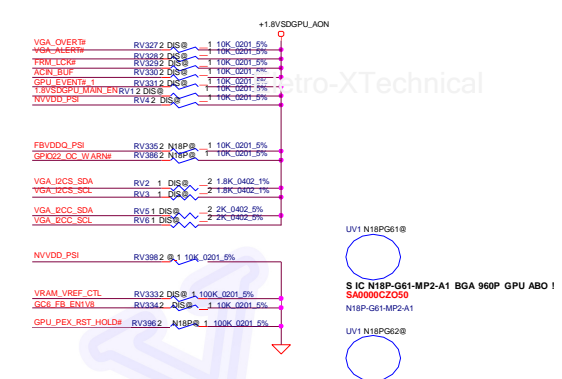
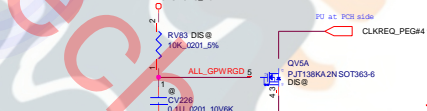
Title	Compal Electronics, Inc.	
	DDR4 DIMMA	
Serial Number	FH5VQM/BLA-J812P	





For nVidia VRAM
N18P-G61-MP2-A1 (Device ID: 1F99)
N18P-G62-A1 (Device ID: 1F95)

Strap/Vendor/Size	Memory PN R3(ABOI)	STRAP[2:0]	Note
 ZZZ X78_L01@ 0x01_Micron_256M x32 X7868B0LO1	 UV4 X78_M4G@ UV6 X78_M4G@ UV5 X78_M4G@ UV7 X78_M4G@ S IC D6 MT61K256M32JE-14: A 1.2V ABO I SA0000BND80	STRAP 2 (H: RV28, L: RV36) STRAP 1 (H: RV27, L: RV35) STRAP 0 (H: RV26, L: RV34)  RV26 X78_M4G@ RV35 X78_M4G@ RV36 X78_M4G@ 100K_0402_5% SD028100380	100K_0201_5% SD043100380
 ZZZ X78_L03@ 0x00_Samsung_256M x32 X7868B0LO3	 UV4 X78_S4G@ UV5 X78_S4G@ UV6 X78_S4G@ UV7 X78_S4G@ S IC D6 256M32 K4Z80325BC-HC14 1.2V ABO I SA0000C6280	 RV34 X78_S4G@ RV35 X78_S4G@ RV36 X78_S4G@ 100K_0402_5% SD028100380	100K_0201_5% SD043100380





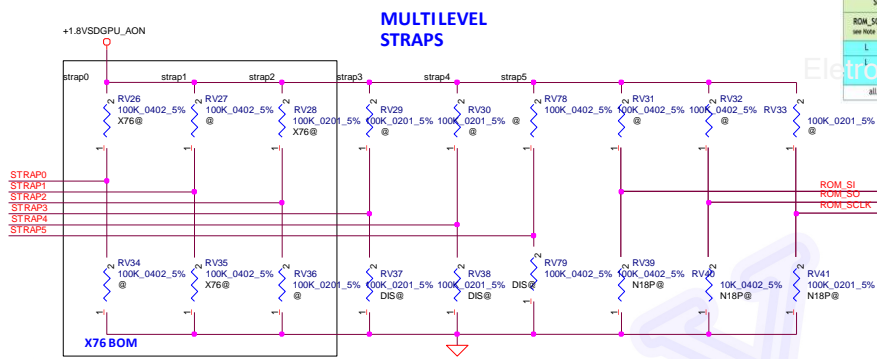
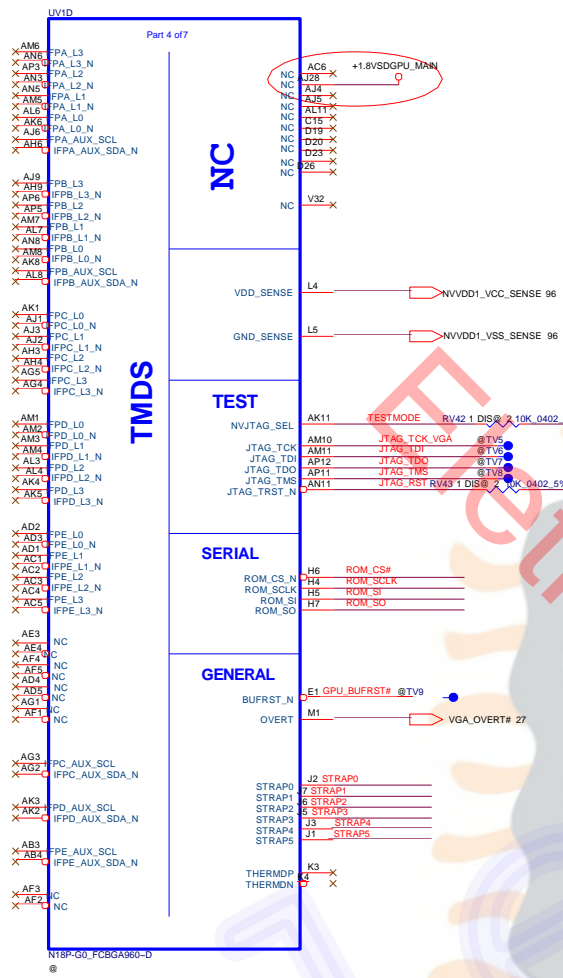


Table 12.4 FS_OVERT* Strap Enable

Strap Pins	see Note 1	FS_OVERT* Function
ROM_SO	see Note 2	FS_OVERT* Function ENABLED
ROM_SI		FS_OVERT* Function DISABLED
ROM_SCLK		FS_OVERT* Function DISABLED
		(do not configure)
		(do not configure)

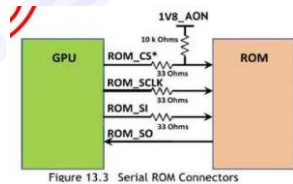


Table 8. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.25V ²	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 ³	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ⁴	Full	Production candidate

- Notes:
- For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
 - DVS is required to run WCLK > 5500 MHz.
 - Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
 - Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.

Table 12.3 RAMCFG

Strap Pins ^{see Note}			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins ^{Note 1}

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ALT_ADDR

LOW	Single GPU
High	Dual GPU

DEVID_SEL

LOW	Orig. Device ID
High	Support G-Sync GPUID

VGA_DEVICE

LOW	3D Device
High	VGA Device

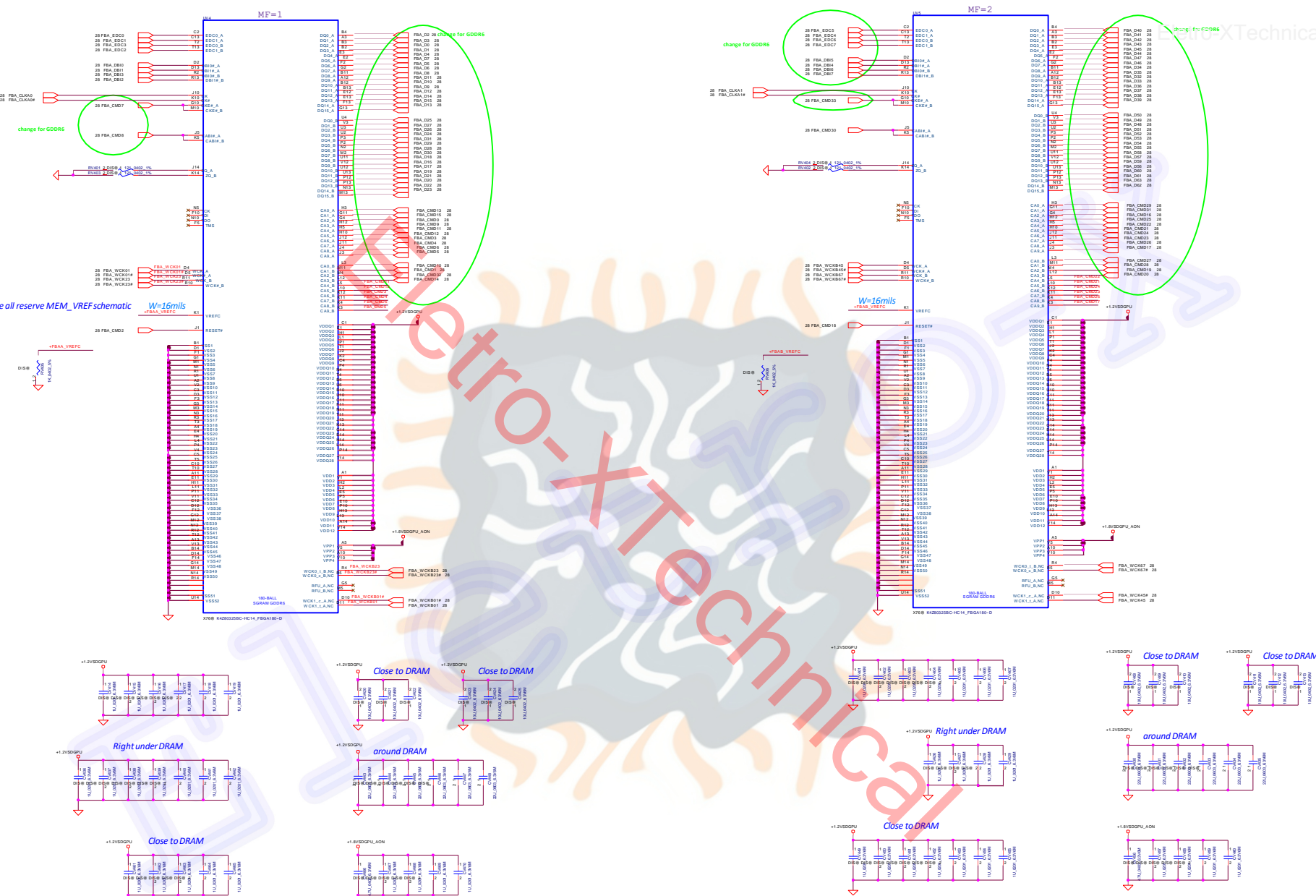
PCIE_CFG

LOW	Normal signal swing
High	Reduce the signal amplitude

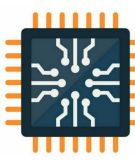
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Issued Date	2019/08/30	Deciphered Date
		2020/08/30

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Title	N18P STRAP3/7
Doc No.	FHSVQ M/B LA-J812P
Rev.	Friday, March 20, 2020
Sheet	29 of 112

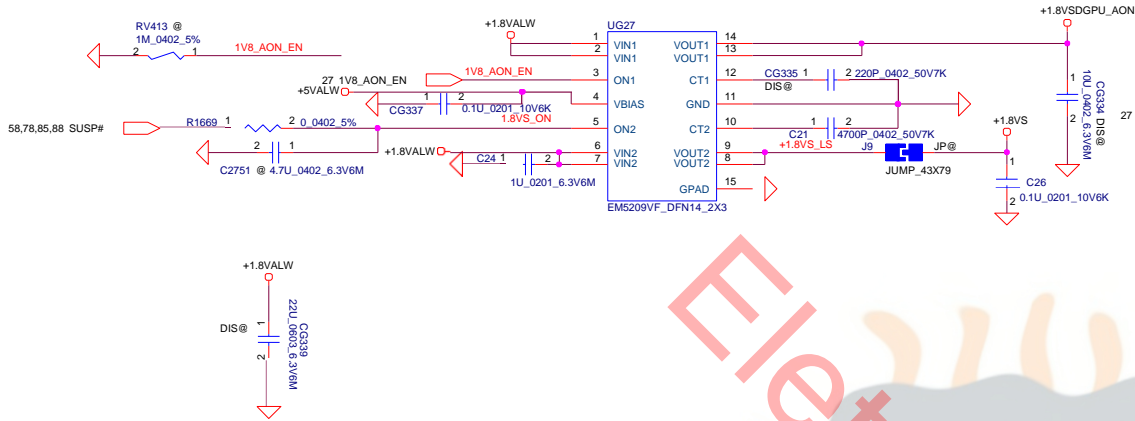


Security Classification		Control Secret Data		Control Secret Data	
Release Date	2019/10/30	Control Secret Data	2020/10/30	Control Secret Data	2020/10/30
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N18P GDDR6 CHA 6/7				FHSVO MB LA-J812P	
COMPAL ELECTRONICS, INC.				1A	

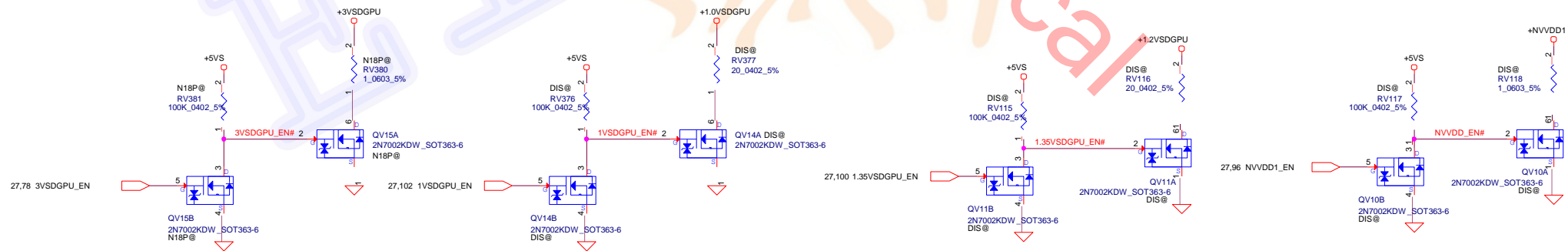
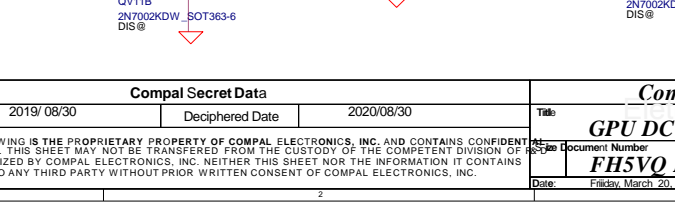
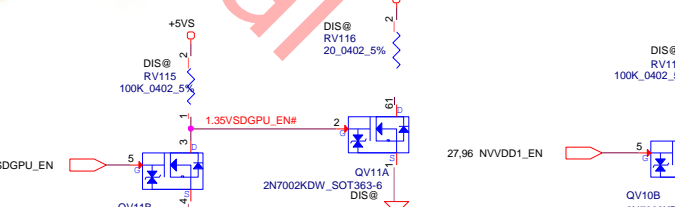
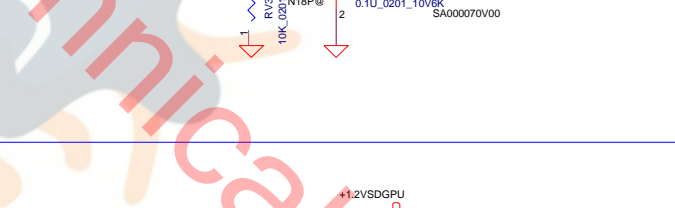
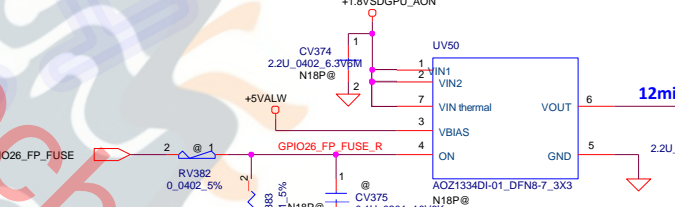
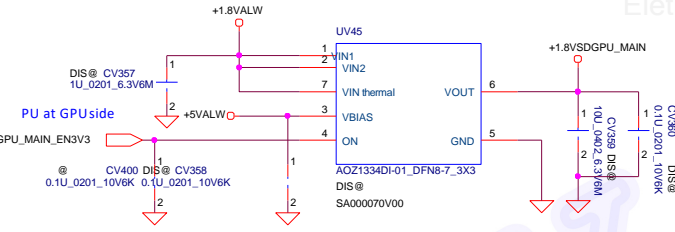




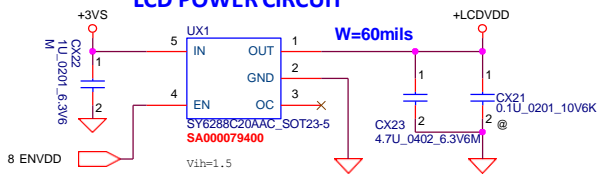
+1.8V_AON/+1.8VS



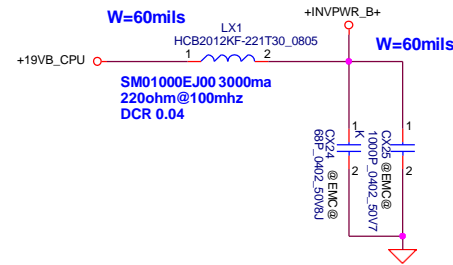
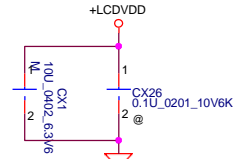
+1.8V_MAIN



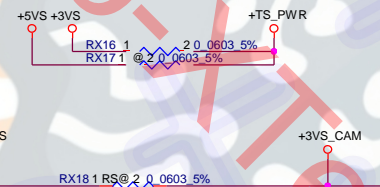
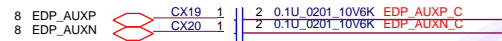
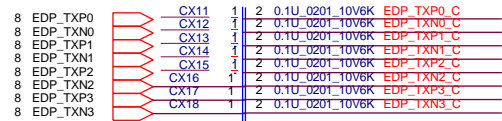
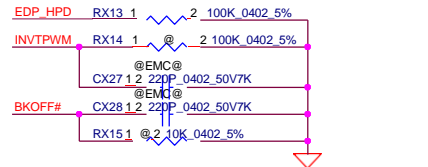
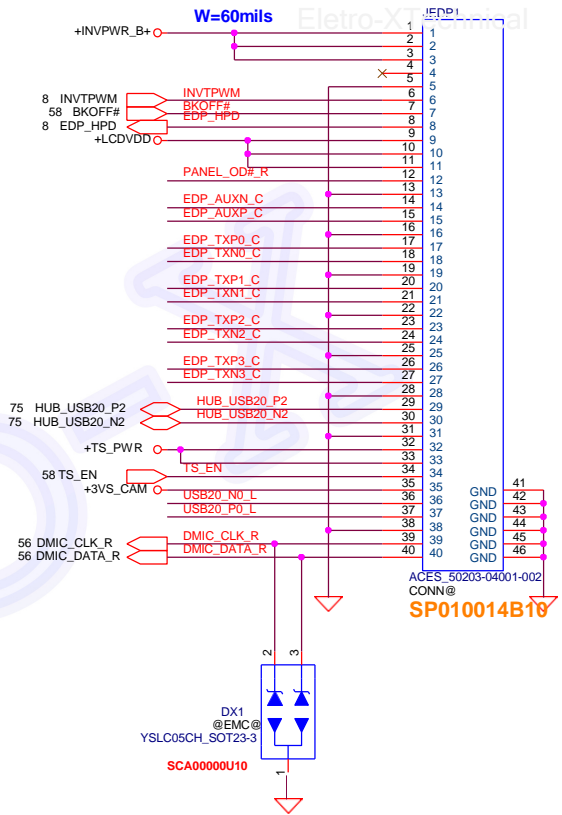
LCD POWER CIRCUIT



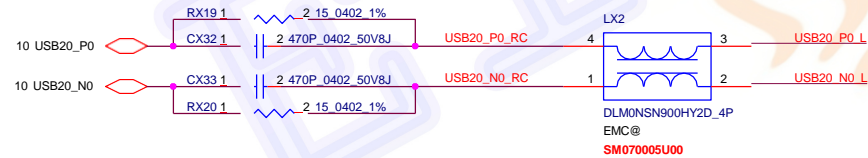
Place closed to JEDP1



LED PANEL Conn.

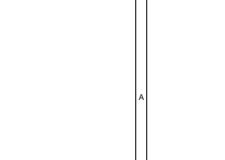
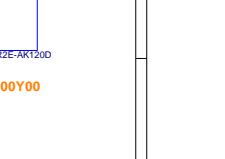
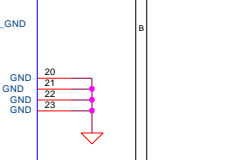
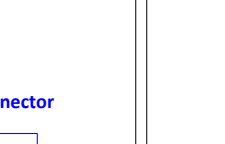
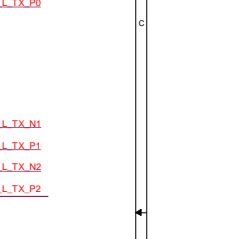
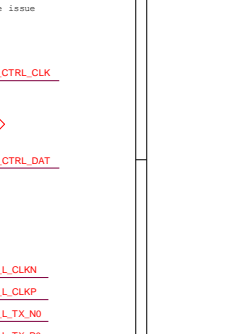
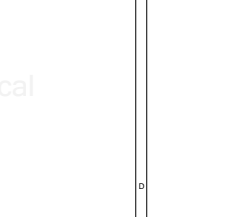
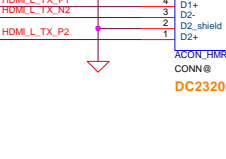
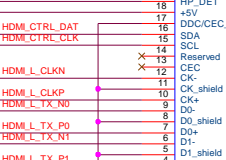
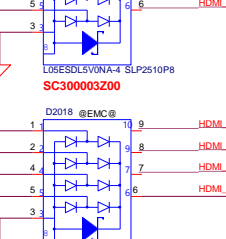
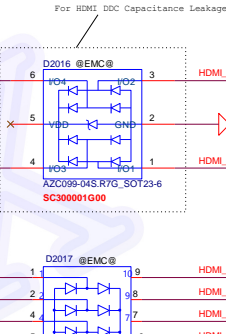
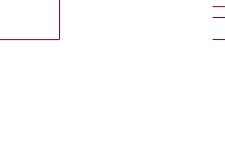
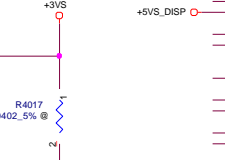
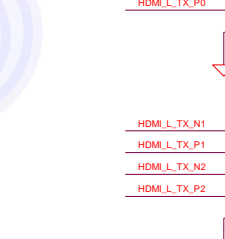
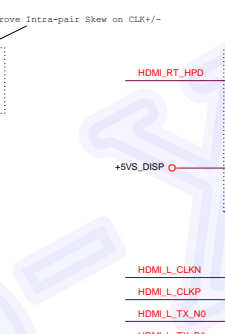
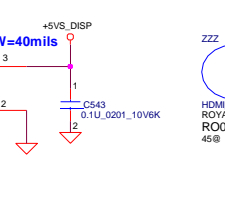
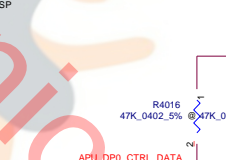
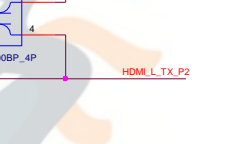
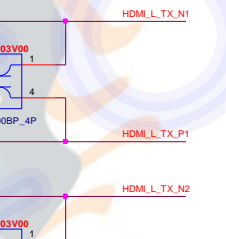
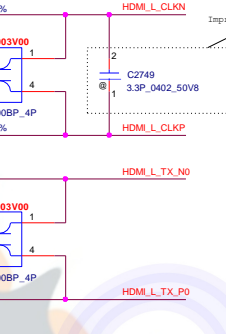
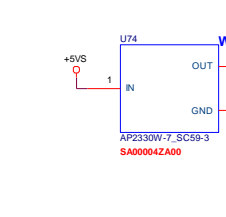
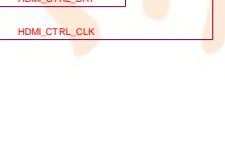
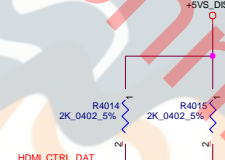
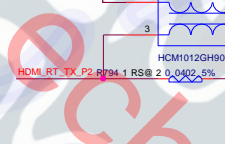
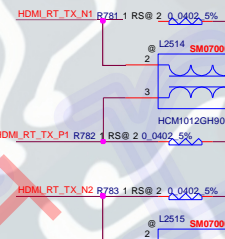
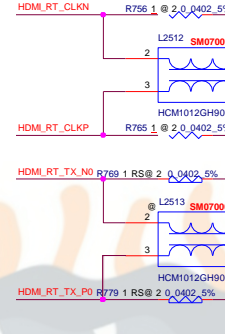
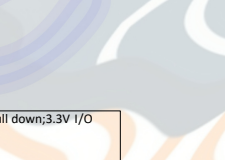
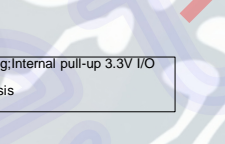
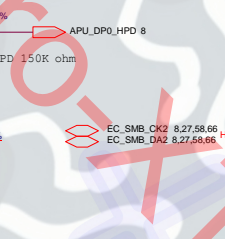
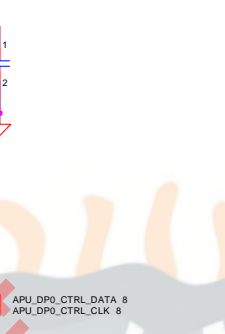
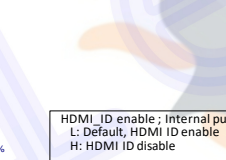
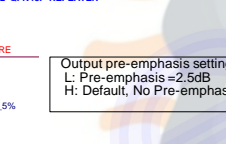
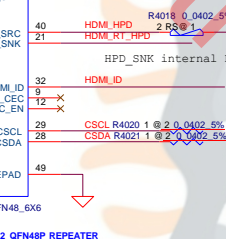
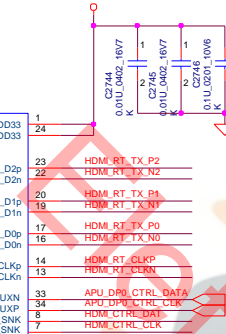
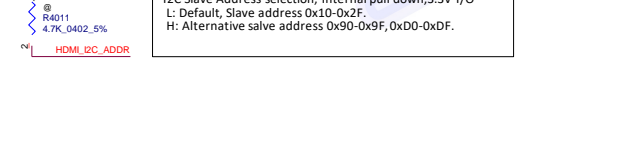
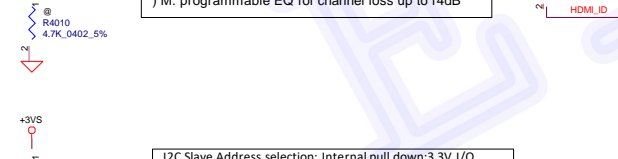
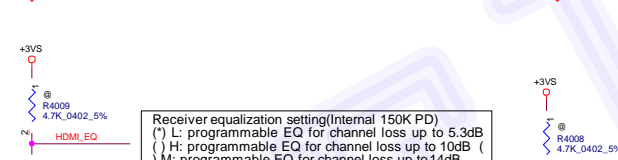
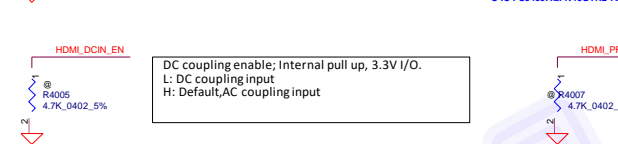
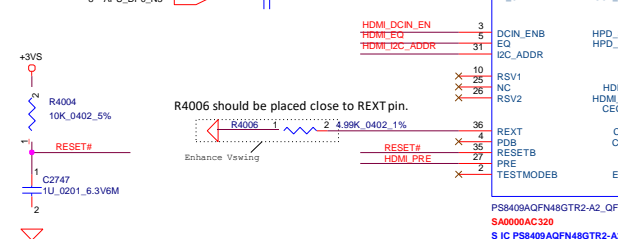
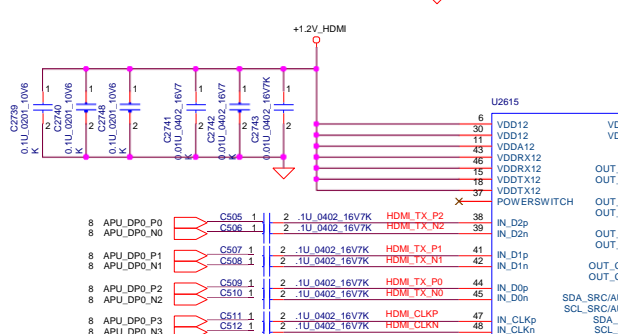
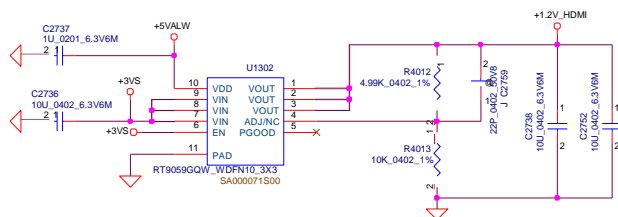


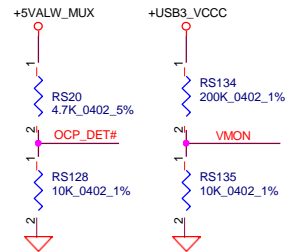
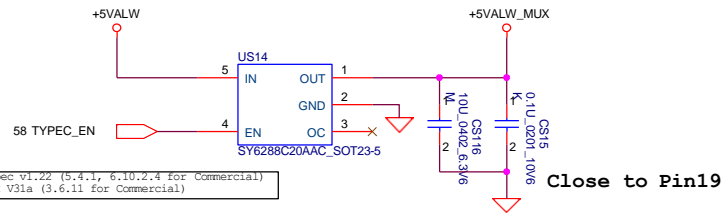
Place closed to JEDP1



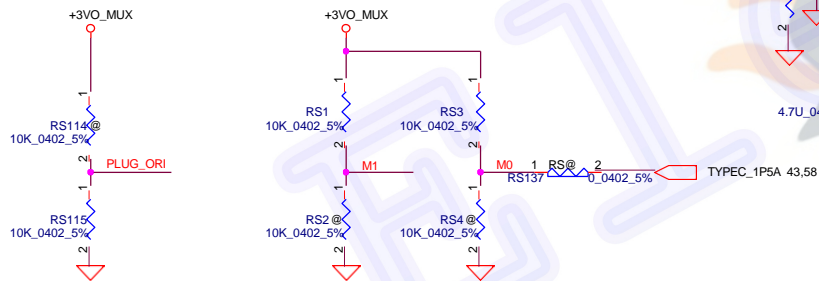
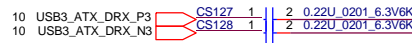
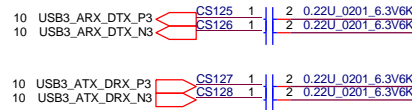
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Date		Friday, March 20, 2020	
Sheet		38 of 40	





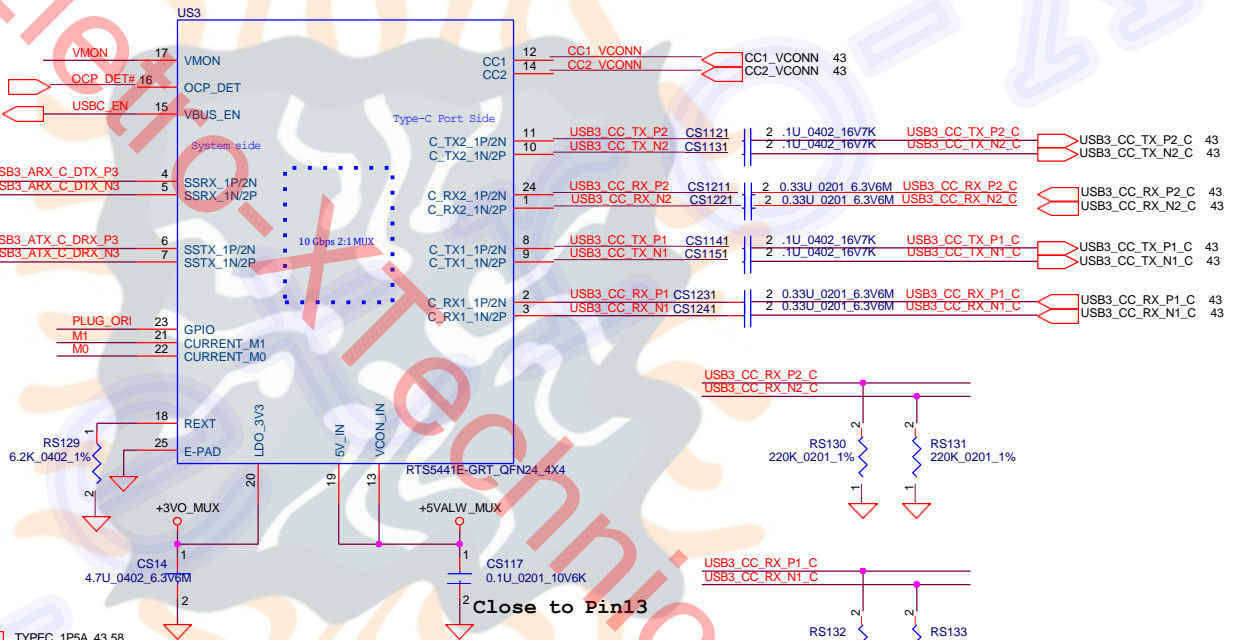
USB3.0 (Port 3)



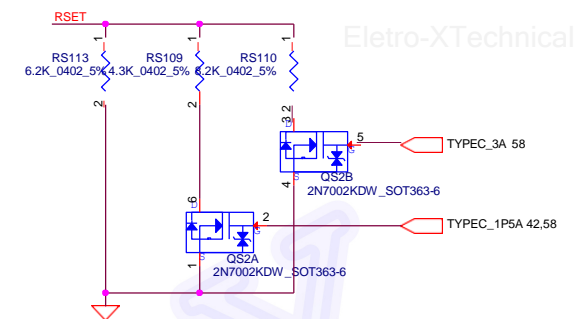
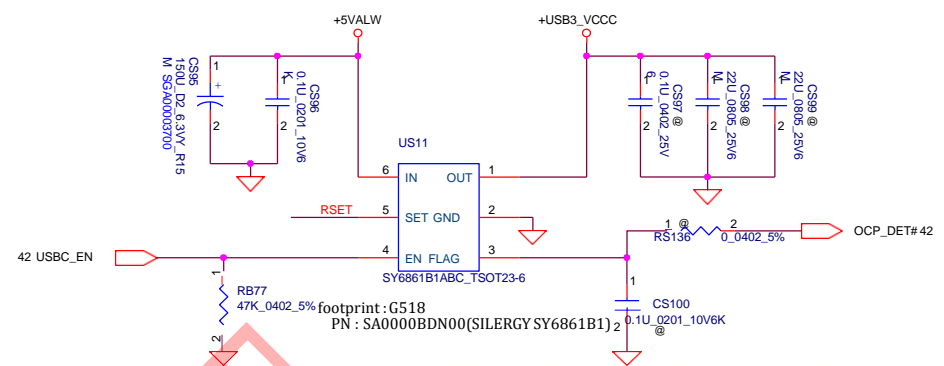
5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery>30%
L	1.5A	1.92A	Battery <30% when DC mode

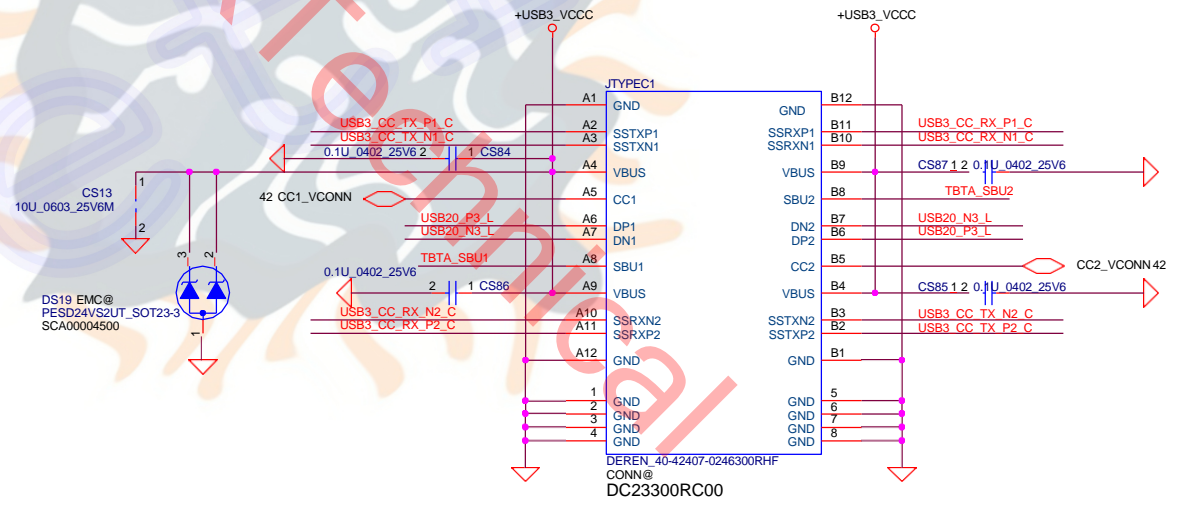
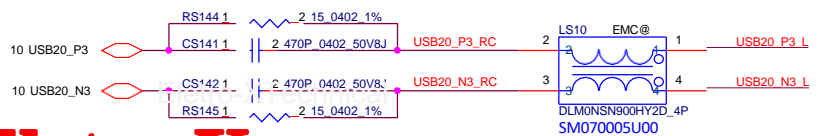
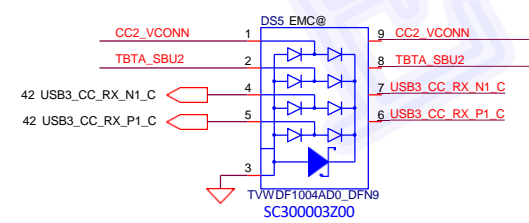
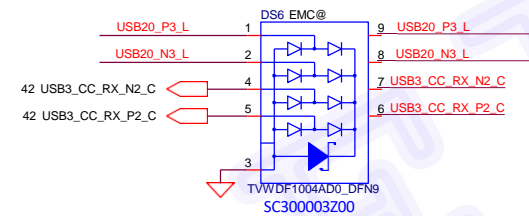
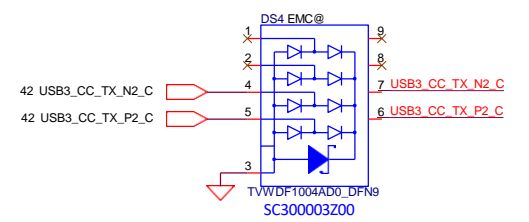
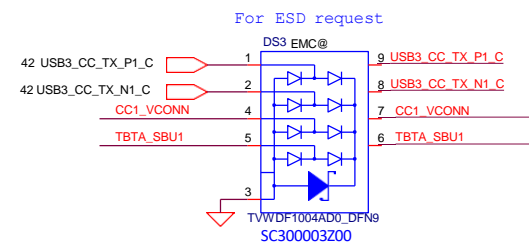
confirm realtek hand-shake



Close to Pin13

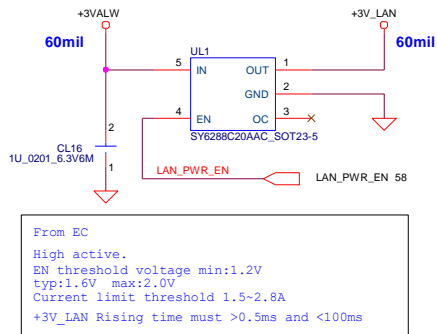


SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limitpoint
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1_VCONN & CC2_VCONN need 20mil trace width.

+3V_LAN Rising time (10%~90%) must >0.5mS and <100mS



RTL8111H LDO mode
RTL8118ASA SWR mode

W=60mil



IDL=1200mA

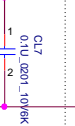
Using for Switch mode

The trace length from Lx to PIN48 (REGOUT) and from C to Lx must < 200mils.

11/27: P/N change to SH00000RT00
(S COIL 2.2UH +20%
HPC252012NF-2R2M 1.3A)

W=60mil

300mA

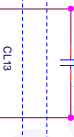


Place near Pin 3,8,22,30

Place near Pin 22

Place near Pin 11,32

W=60mil

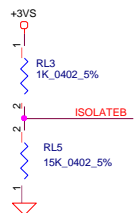


Place near Pin 11,32

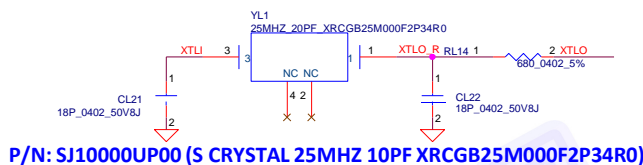
Using for Switch mode

The trace length from C to PIN46,47(VDDREG) must < 200mils.

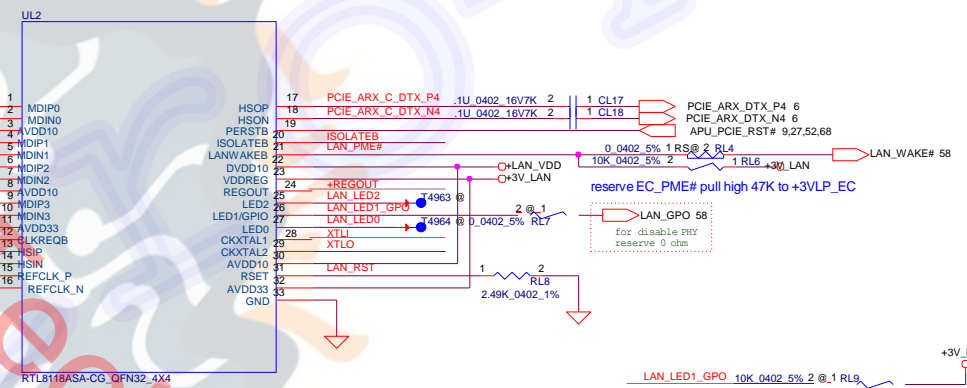
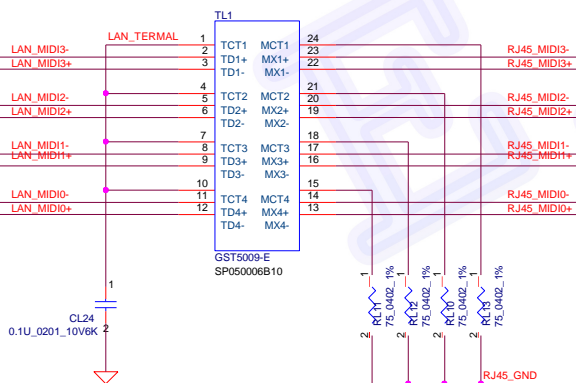
Reserve for surge improvement
Place near Pin 11,32



LAN_CLKREQ# pull up at PCHside

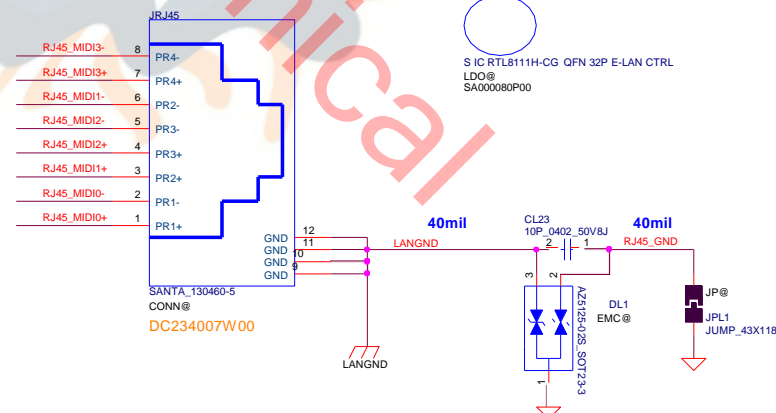


P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



RTL8118ASA-CG, QFN32_4x4
SA0000B9F20
SWR@
SA0000B9F20, S IC RTL8118ASA-CG QFN 32P E-LAN CTRL

LAN Connector

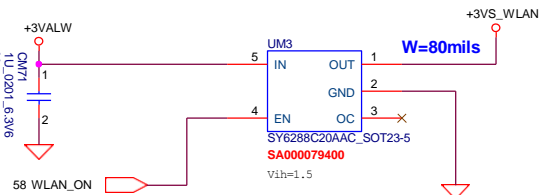
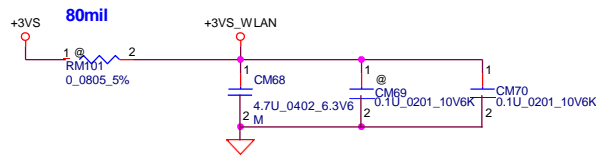


Eleto-XTechnical

Eleto-X

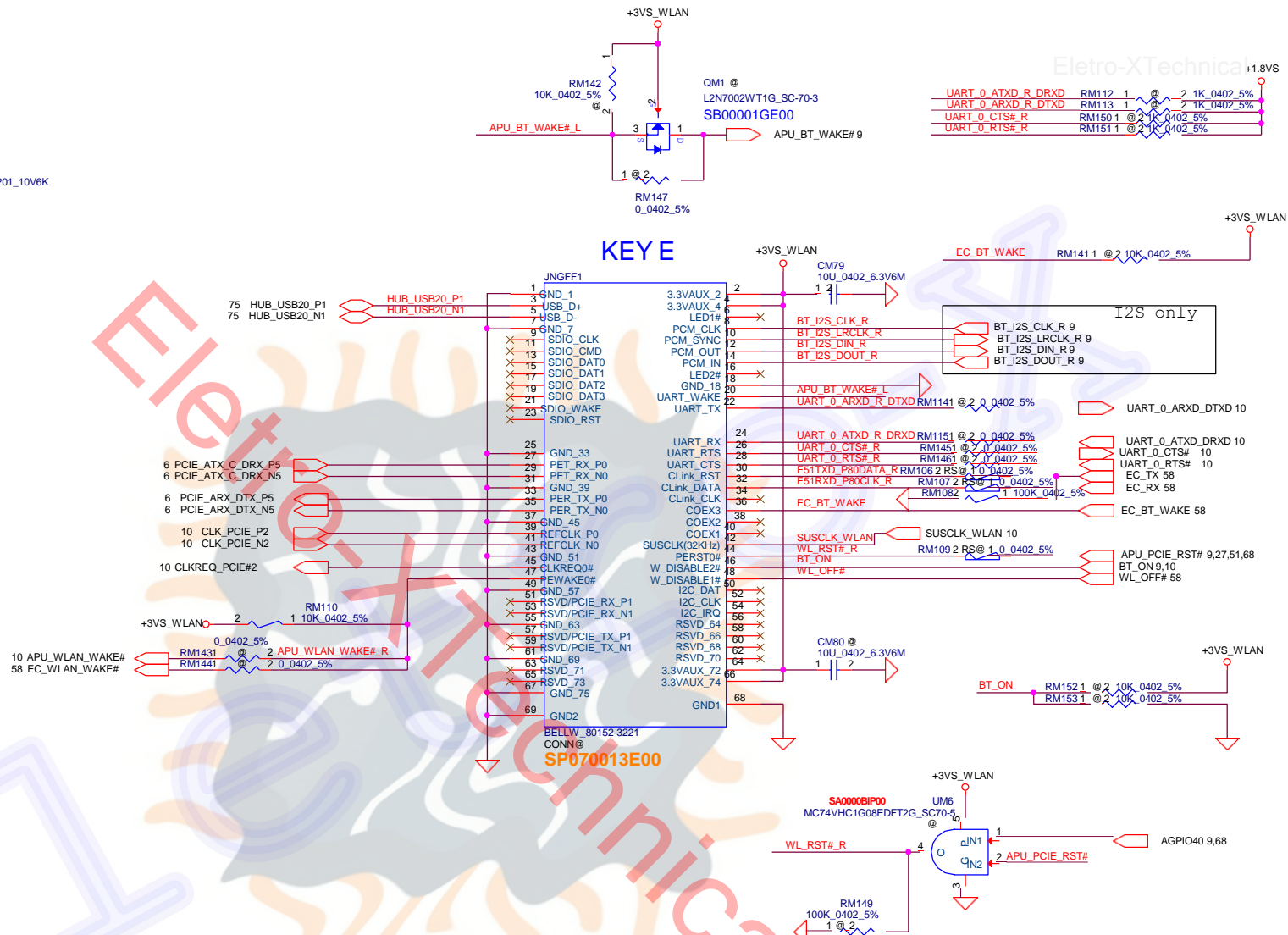
Security Classification			Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/08/30	Deciphered Date	2020/08/30	Title	LAN RTL8111H	
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				Date:	Fri, Mar 20, 2020	Sheet 51 of 51

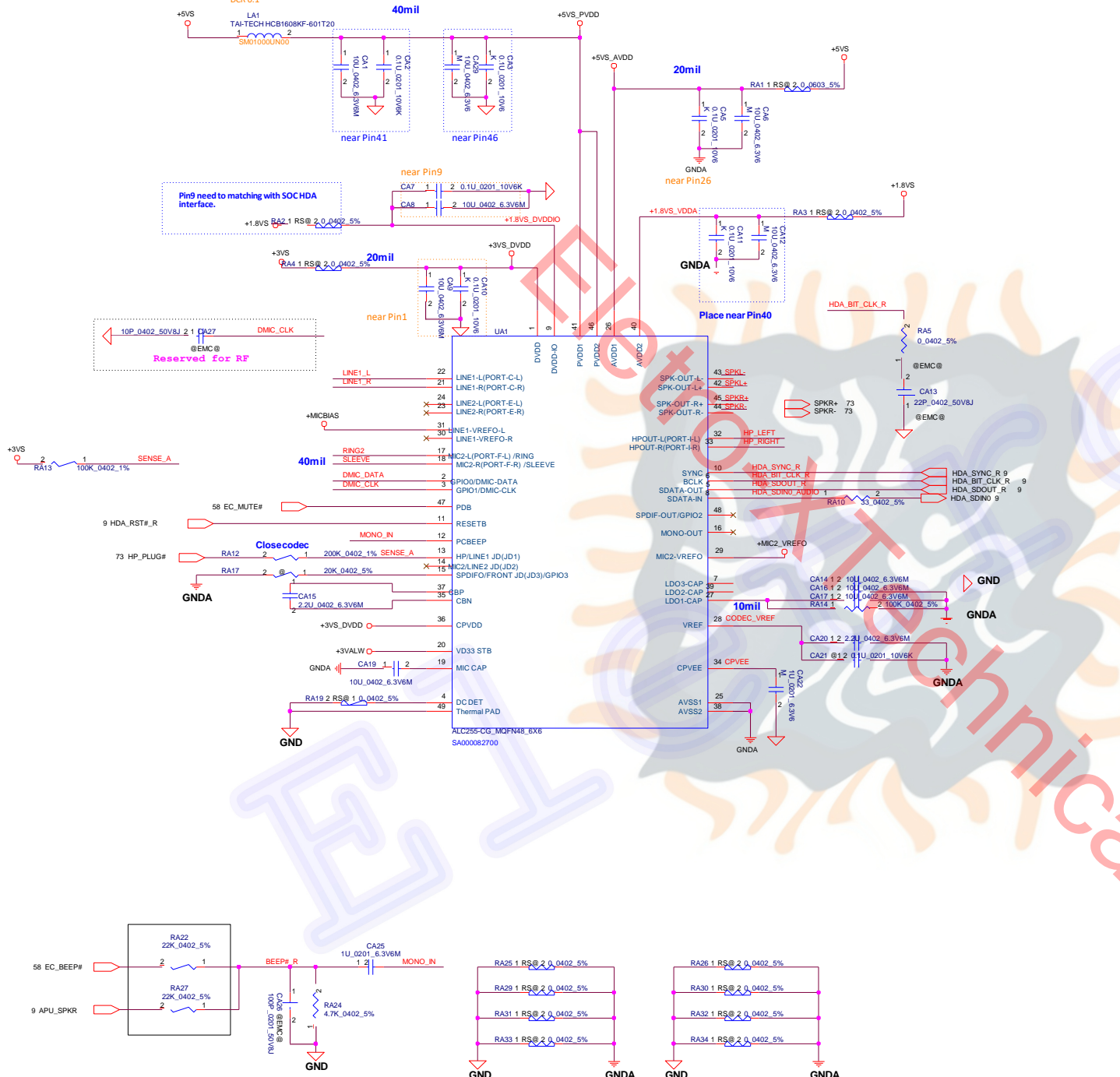
Wireless LAN



NGFF WL+BT (KEY E)

74	U0	GND	75
72	U0	RESERVED/REFCLKN1	73
70	UM_Power_SPC/GPIO/PEWake3a	RESERVED/REFCLKP1	71
68	UM_Power_SNM/CLKREQ1a	GND	69
66	UM_SWP/PERST1a	Reserved/PERn1	67
64	RESERVED	Reserved/PERn0	65
62	ALERT# (IO)(0.3.V)	GND	63
60	QC CLK (IO)(0.3.V)	Reserved/PETn1	61
58	QC DATA (IO)(0.3.V)	Reserved/PETp1	59
56	W_DISABLEB1 (O)(0.3.V)	GND	57
54	Reserved/W_DISABLEB2 (O)(0.3.V)	PEWakeB1 (O)(0.3.V)	55
52	PERST0 (O)(0.3.V)	CLKREQD1 (O)(0.3.V)	53
50	SUSCIN(32H) (O)(0.3.V)	GND	51
48	CODK1 (IO)(0.1.8V)	REFCLKNO	49
46	CODK2 (IO)(0.1.8V)	REFCLKPO	47
44	CODK3 (IO)(0.1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (IO)(0.1.8V)	PETn0	37
34	UART CTS (IO)(0.1.8V)	PETp0	35
32	UART Tx (IO)(0.1.8V)	CLKREQD	33
22	UART Rx (IO)(0.1.8V)	SIOD Resistor (O)(0.1.8V)	23
20	UART Wake (IO)(0.3.V)	SIOD WakeB1 (IO)(0.1.8V)	21
18	GND	SIOD DATA (IO)(0.1.8V)	19
16	LED2# (IO)(O)	SIOD DATA (IO)(0.1.8V)	17
14	PCM_OUT/IS_SD_OUT (IO)(0.1.8V)	SIOD DATA (IO)(0.1.8V)	15
12	PCM_IN/IS_SD_IN (IO)(0.1.8V)	SIOD DATA (IO)(0.1.8V)	13
10	PCM_SYNC/IS WS (IO)(0.1.8V)	SIOD CMDB (IO)(0.1.8V)	11
8	PCM_CLK/IS SCK (IO)(0.1.8V)	SIOD CLKO (IO)(0.1.8V)	9
6	LED1# (IO)(O)	GND	7
4	U0	UM_D_	5
2	U0	UM_D_+	3
		GND	1



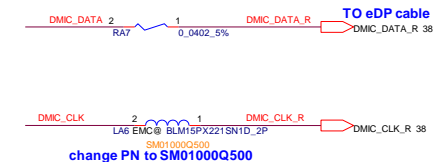


Int. Speaker Conn.

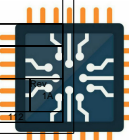
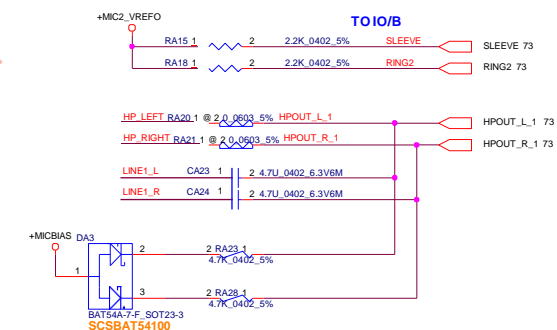


Digital MIC

MIC BOM upload by Audio Team

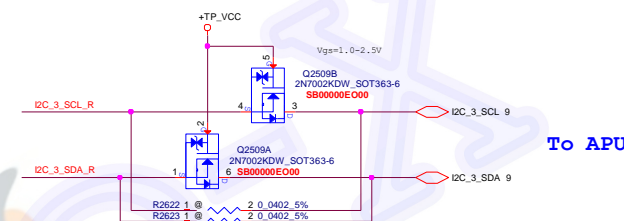
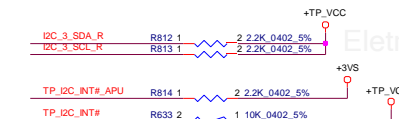
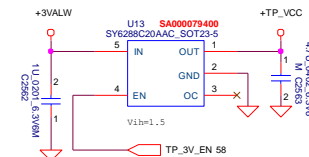
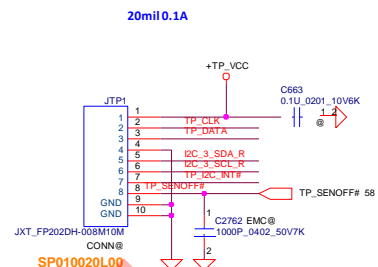
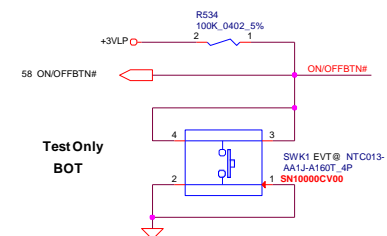


Headphone Out

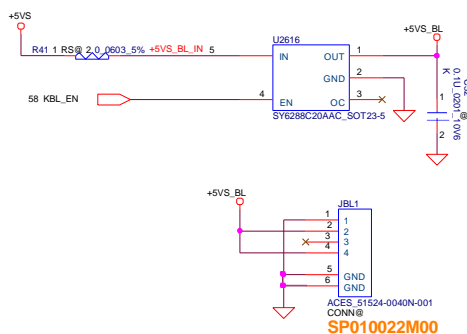


ON/OFF BTN

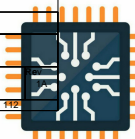
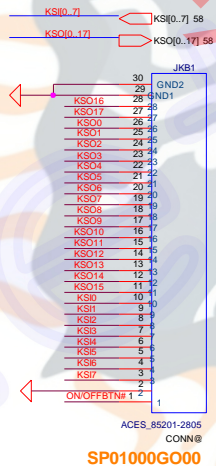
TP/B Conn.



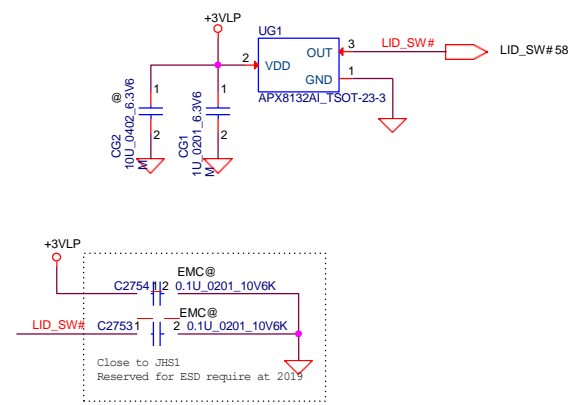
KB Backlight



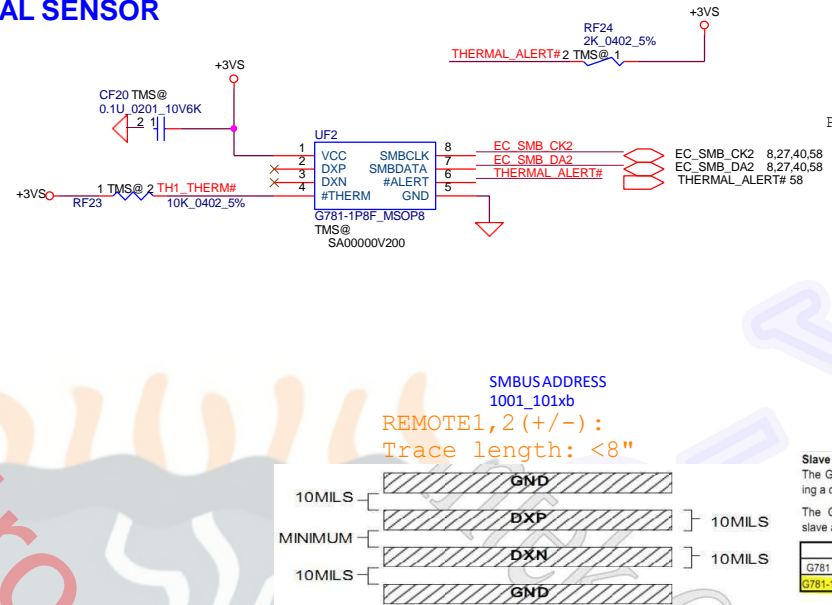
KB Conn.



Hall sensor

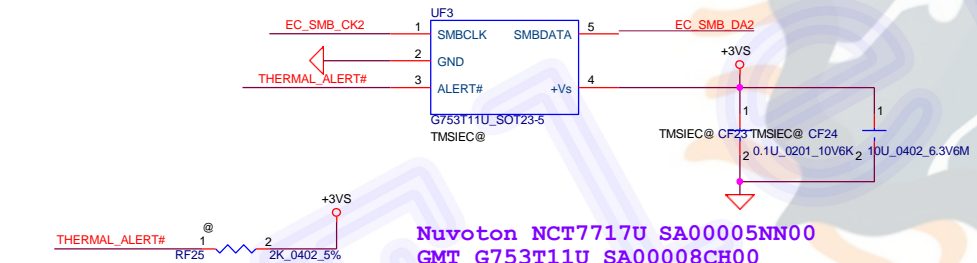


THERMAL SENSOR



THERMAL SENSOR IEC safety

Finger Print



Power Source Check

EGIS ETU801 +FP VCC=5V

ELAN FA6780-220 +FP VCC=3.3V

PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

PULL-UP RESISTOR	TEMPERATURE (°C)
2kΩ	75
7.5kΩ	90
10.5kΩ	100
14kΩ	105
18.7kΩ	110

6.3 Address Setting

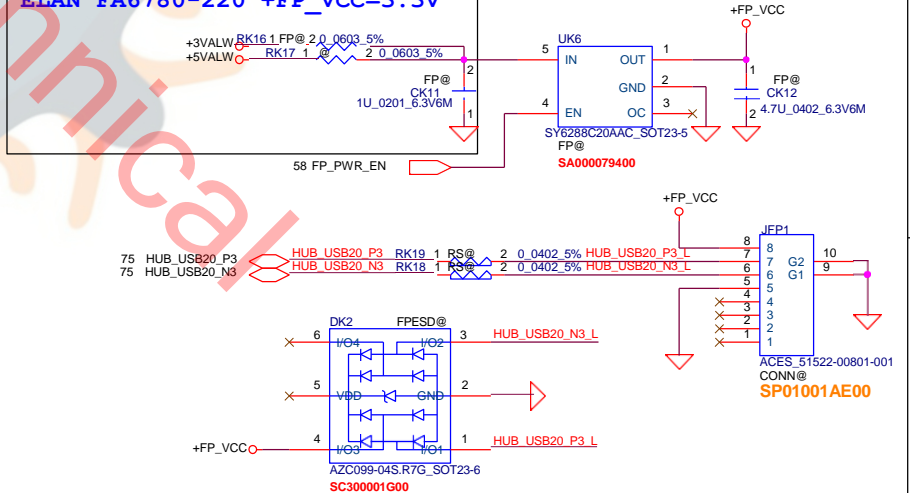
NCT7717U I²C/ SMBus™ address is 1001000xb (x is R/W bit).

Slave Address

The G753 appears to the SMBus as one device having a common address for both ADC channels. The G753 has the following SMBus slave address:

A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0

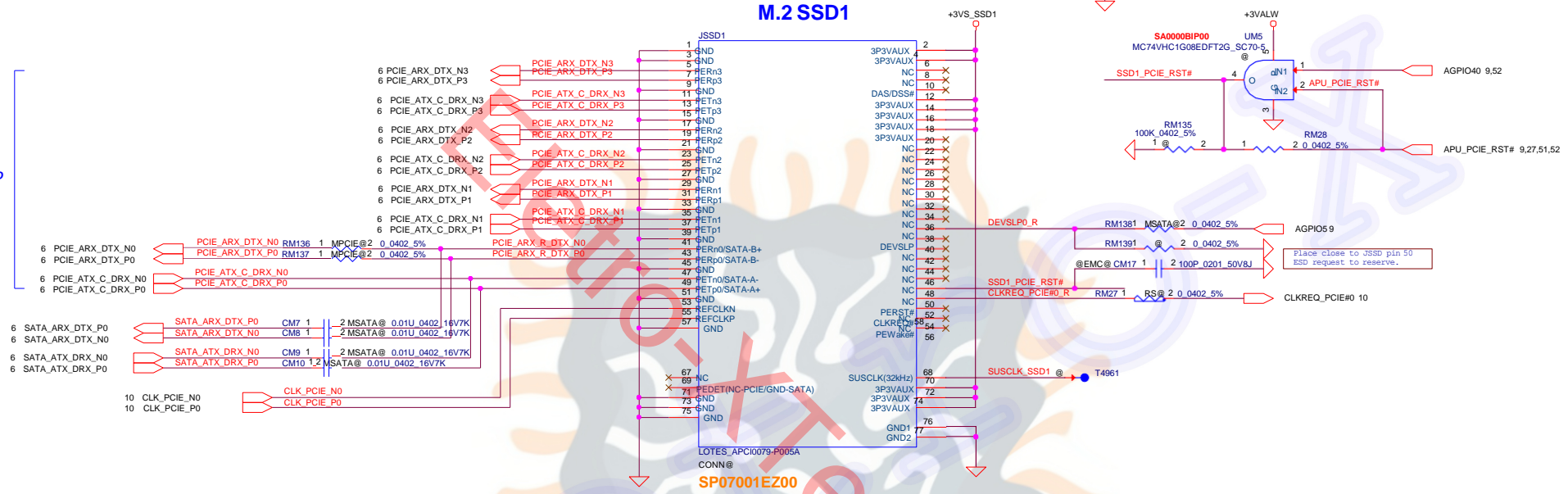
The G753 also responds to the SMBus Alert Response slave address (see the Alert Response Address section).



M.2 PCIe SSD Conn.

M.2 SSD1

PCIE SSD

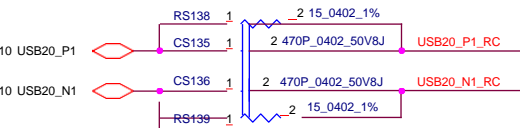


Eletro-XTechnical

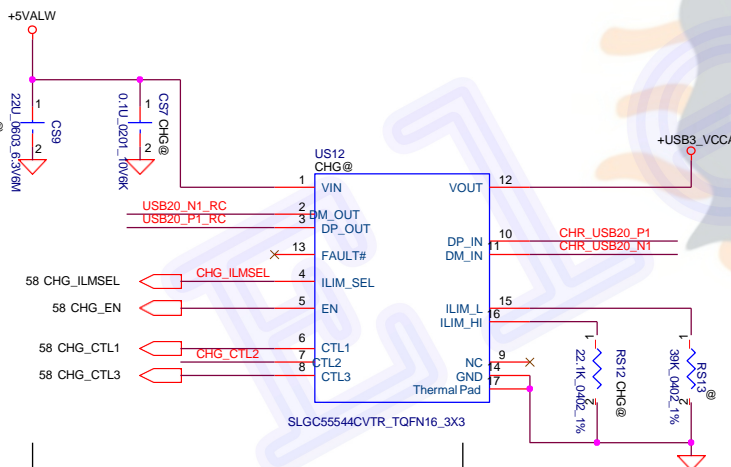
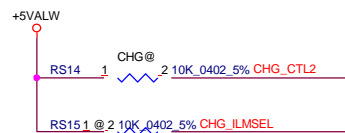
Eletro-X

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				Date:	Friday, March 20, 2020	Sheet 68 of 68

USB3.0



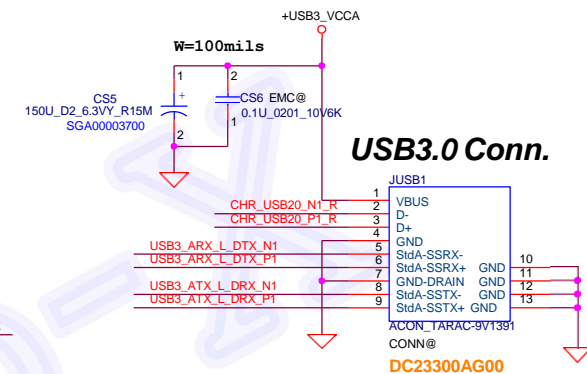
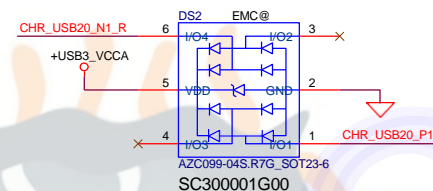
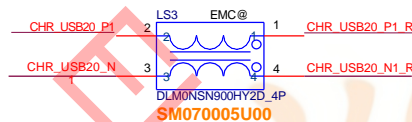
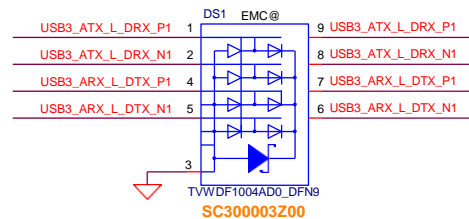
USB Host Charger



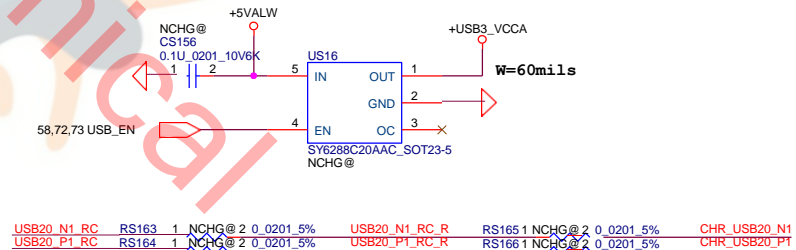
USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Disconnected Data Lines Security

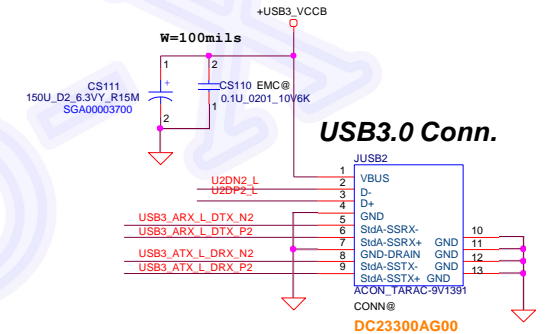
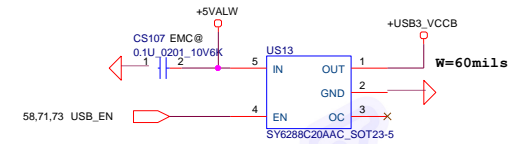
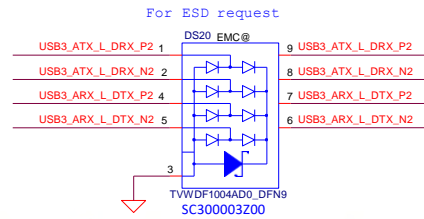
ILM R vaule
 $I_{os} (mA) = 50250 / R (Kohm)$
 $ILIM_Hi = 2273mA$
 $ILIM_L = 1288mA (reserve)$



Reserved for non-Charger



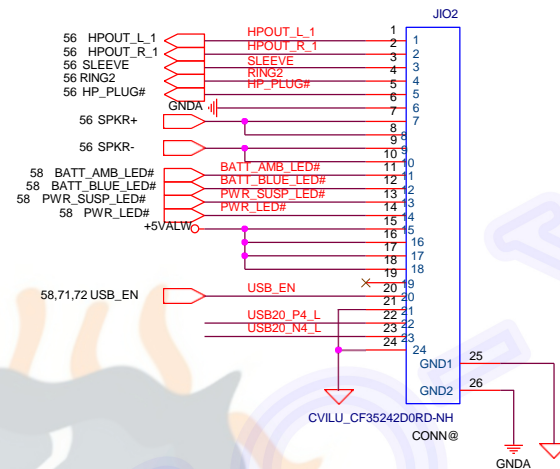
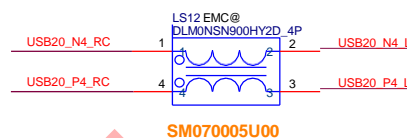
USB3.0



USB3.0 Conn.

IO/B CONN

Eletro-XTechnical

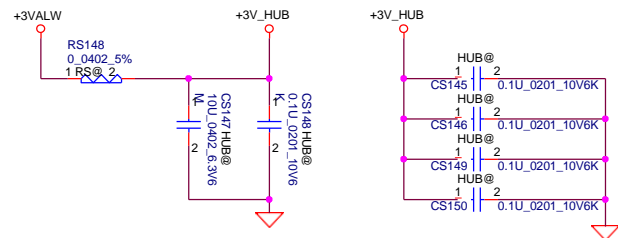


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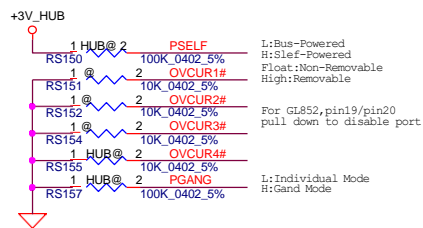
Title		Compal Electronics, Inc.	
IO/B Interface		FH5VQ M/B LA-J812P	
Date:	Friday, March 20, 2020	Sheet	73 of 73



USB HUB



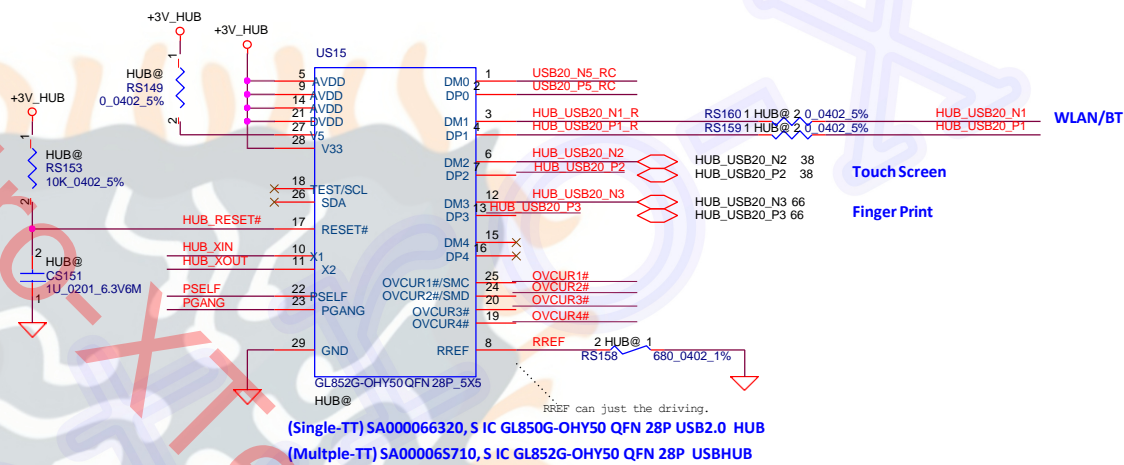
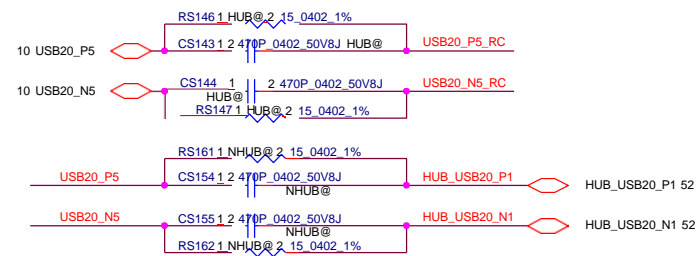
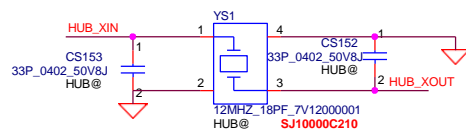
C279 close to U73 pin5
C280 close to U73 pin9
C283 close to U73 pin14
C284 close to U73 pin21



L:Bus-Powered
H:Sleep-Powered
Float:Non-Removable
High:Removable

For GL852, pin19/pin20
pull down to disable port

L:Individual Mode
H:Gand Mode



(Single-TT) SA000066320, S IC GL850G-OHY50 QFN 28P USB2.0 HUB
(Multiple-TT) SA000065710, S IC GL852G-OHY50 QFN 28P USBHUB

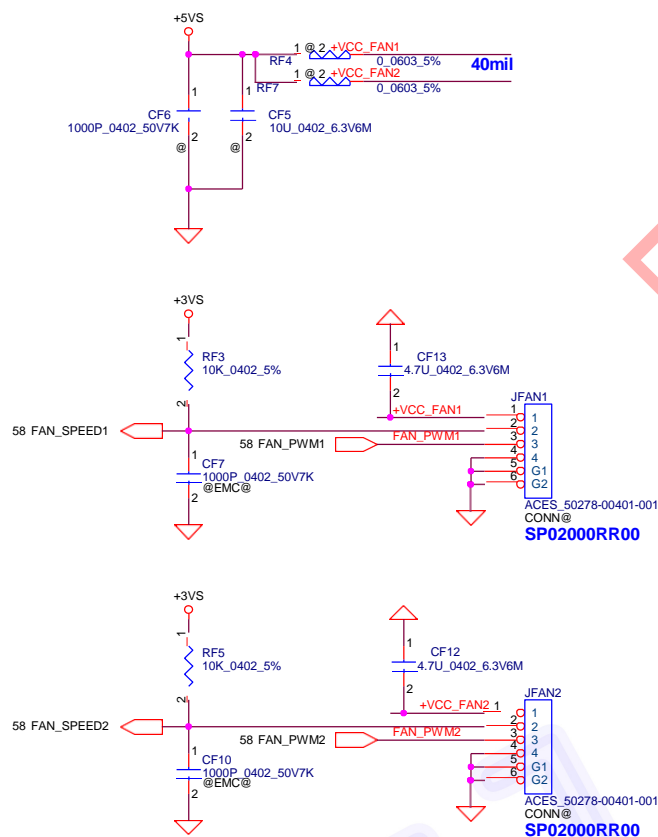
Touch Screen
Finger Print

WLAN/BT

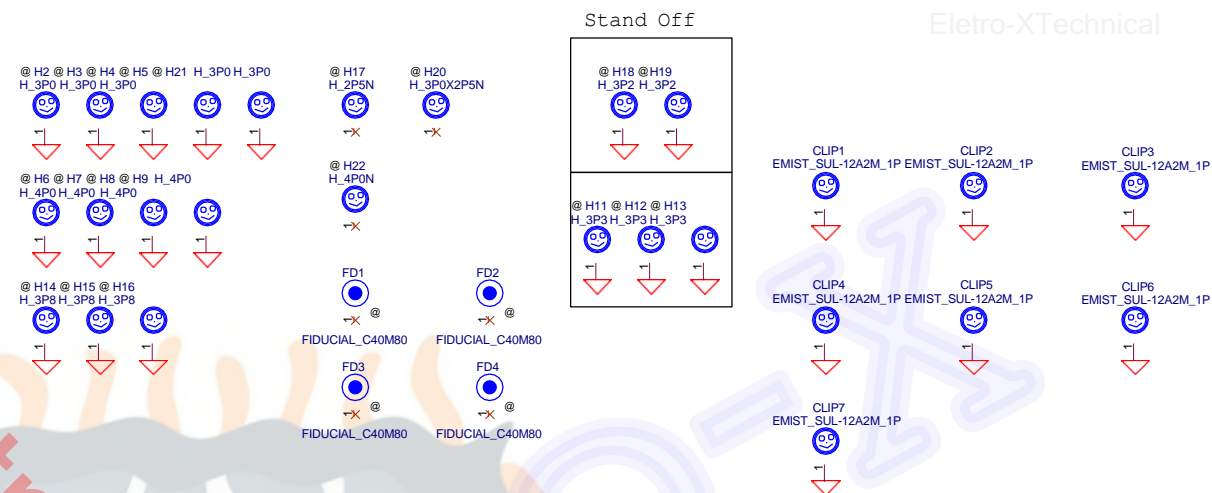
Eletro-XTechnical

Eletro-X

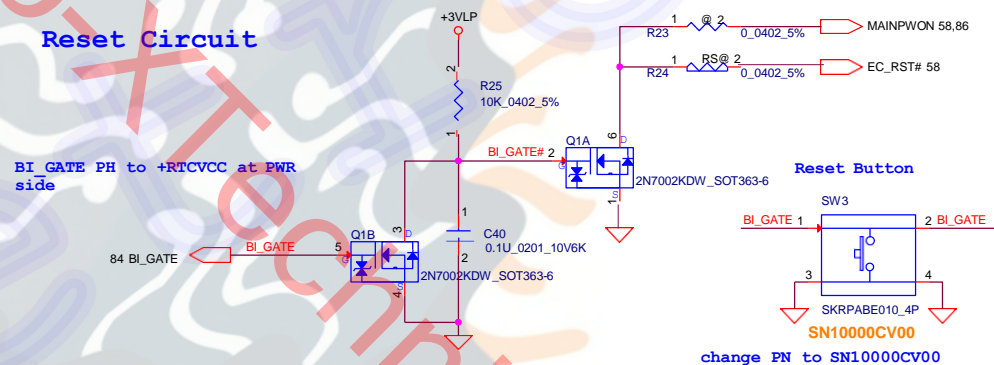
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/ 08/30	Deciphered Date	2020/08/30	Title	USB2.0 HUB
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				Date	Fri Mar 20, 2020
				Sheet	75 of 1



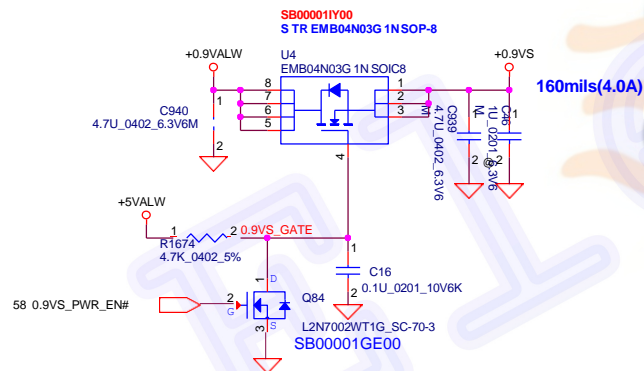
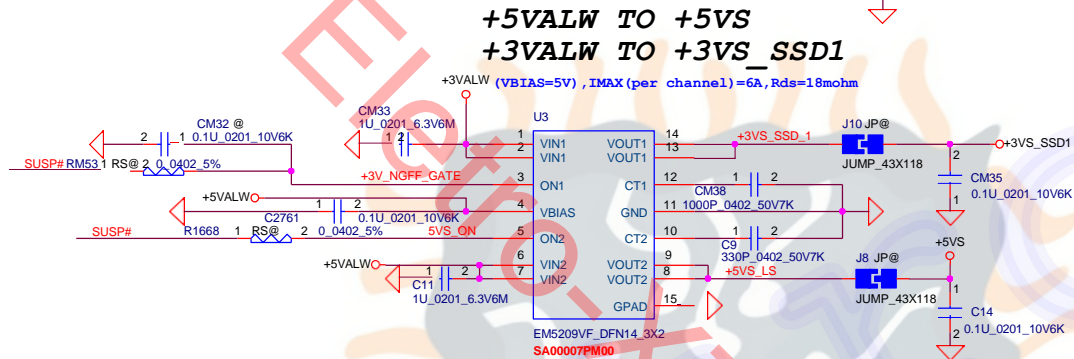
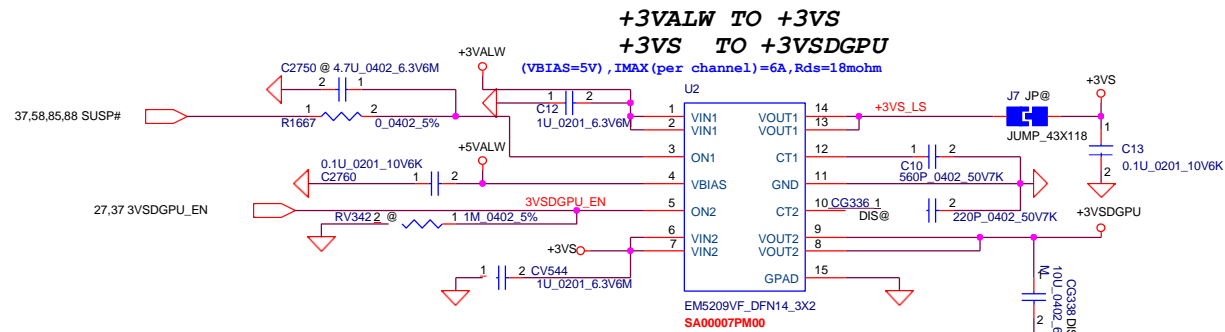
Screw Hole



Reset Circuit

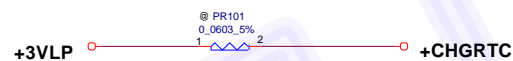
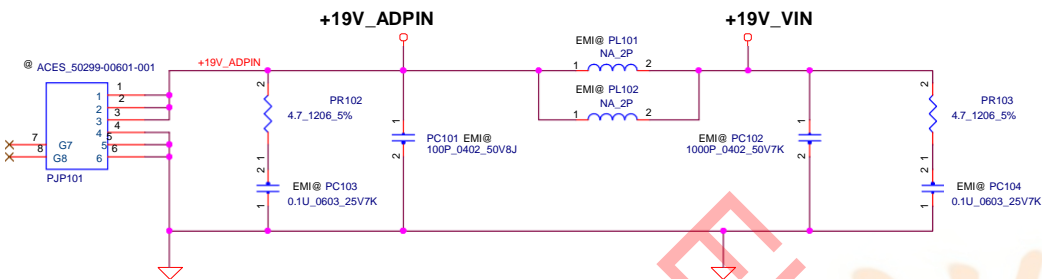


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				Sheet	77 of 112

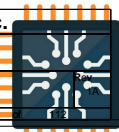


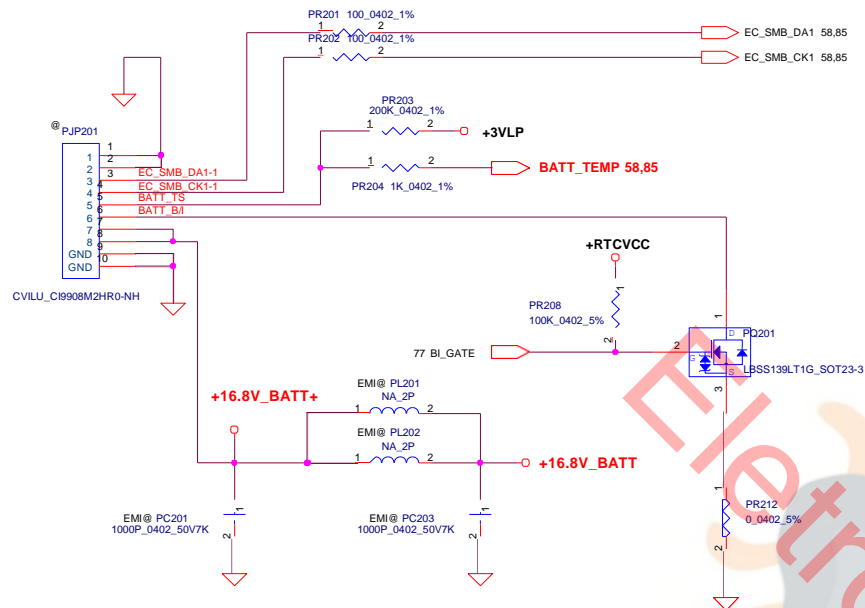
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Issued Date	2019/08/30	Deciphered Date	2020/08/30	Title
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				FH5VQ M/B LA-J812P
				Date: Friday, March 20, 2020
				Sheet 78 of 11



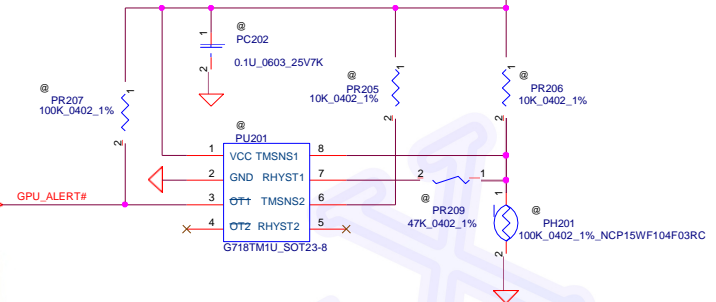


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Sheet	82





58 GPU_ALERT#



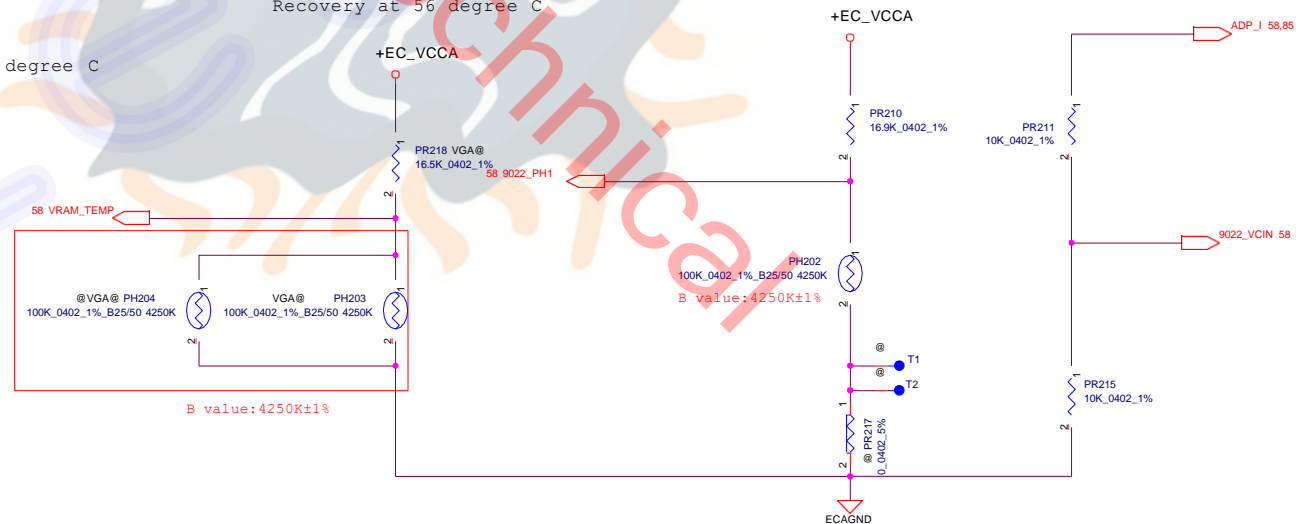
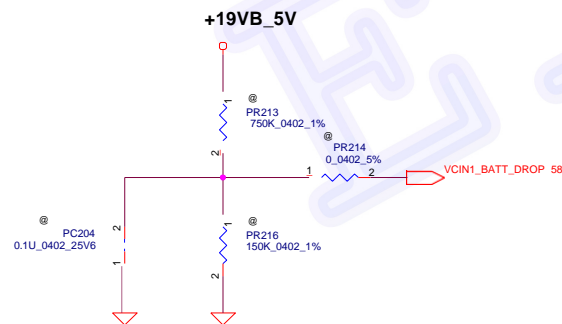
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2.V
PH202 (ohm)	7.3092K	26.11K

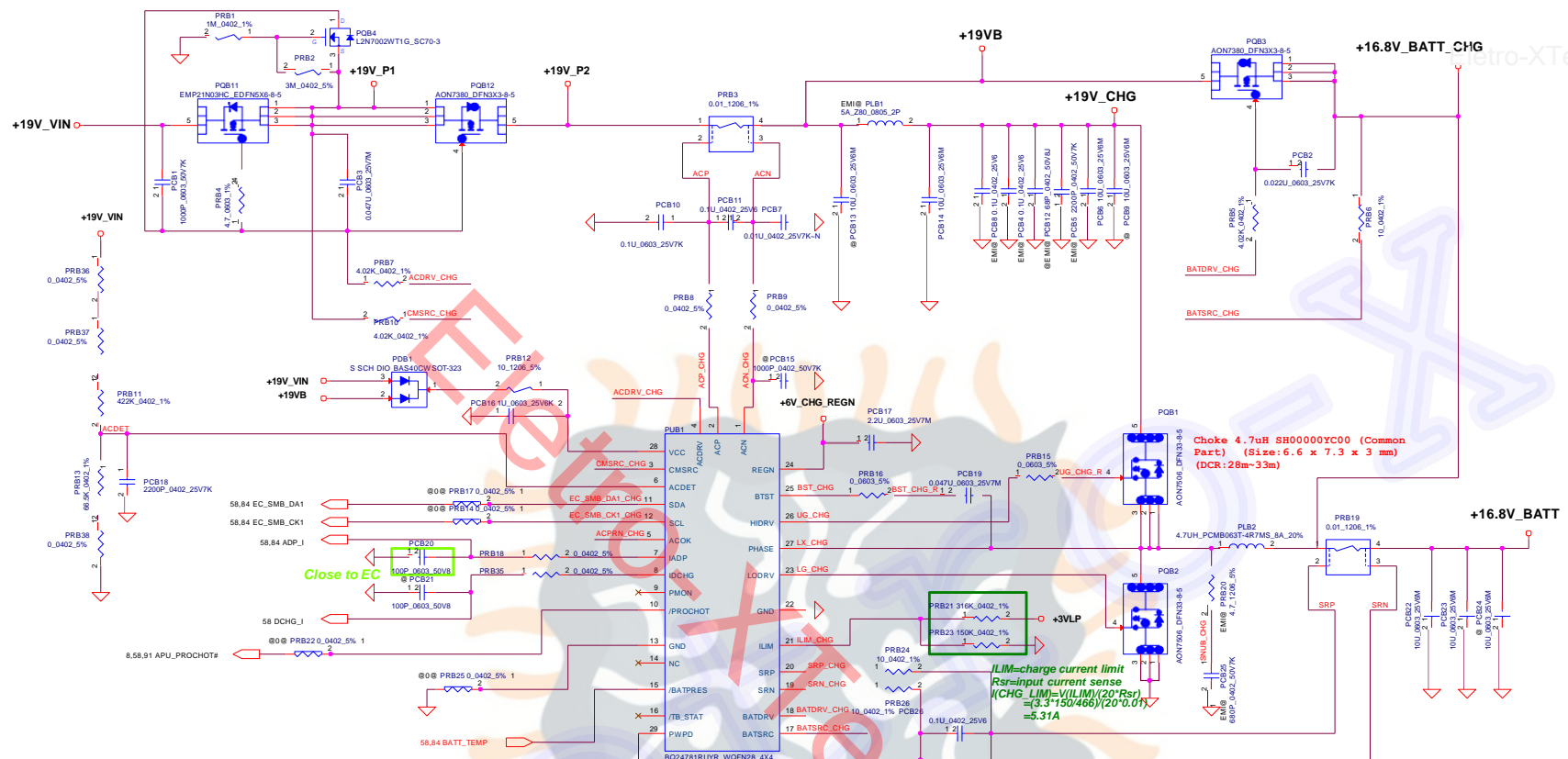
For KB9012 sense 20mG	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C

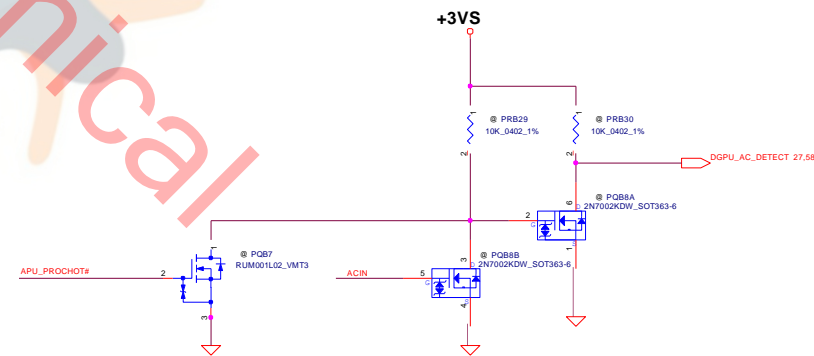
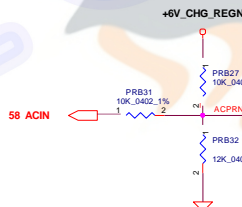
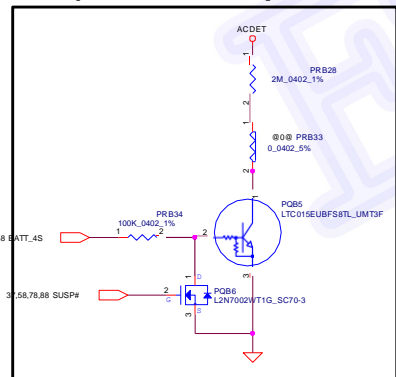
2013/10/02
Add for ENE9022 Battery Voltage drop detection. Recovery at 56 degree C
Connect to ENE9022 pin64 AD1.

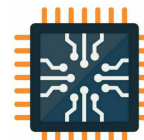
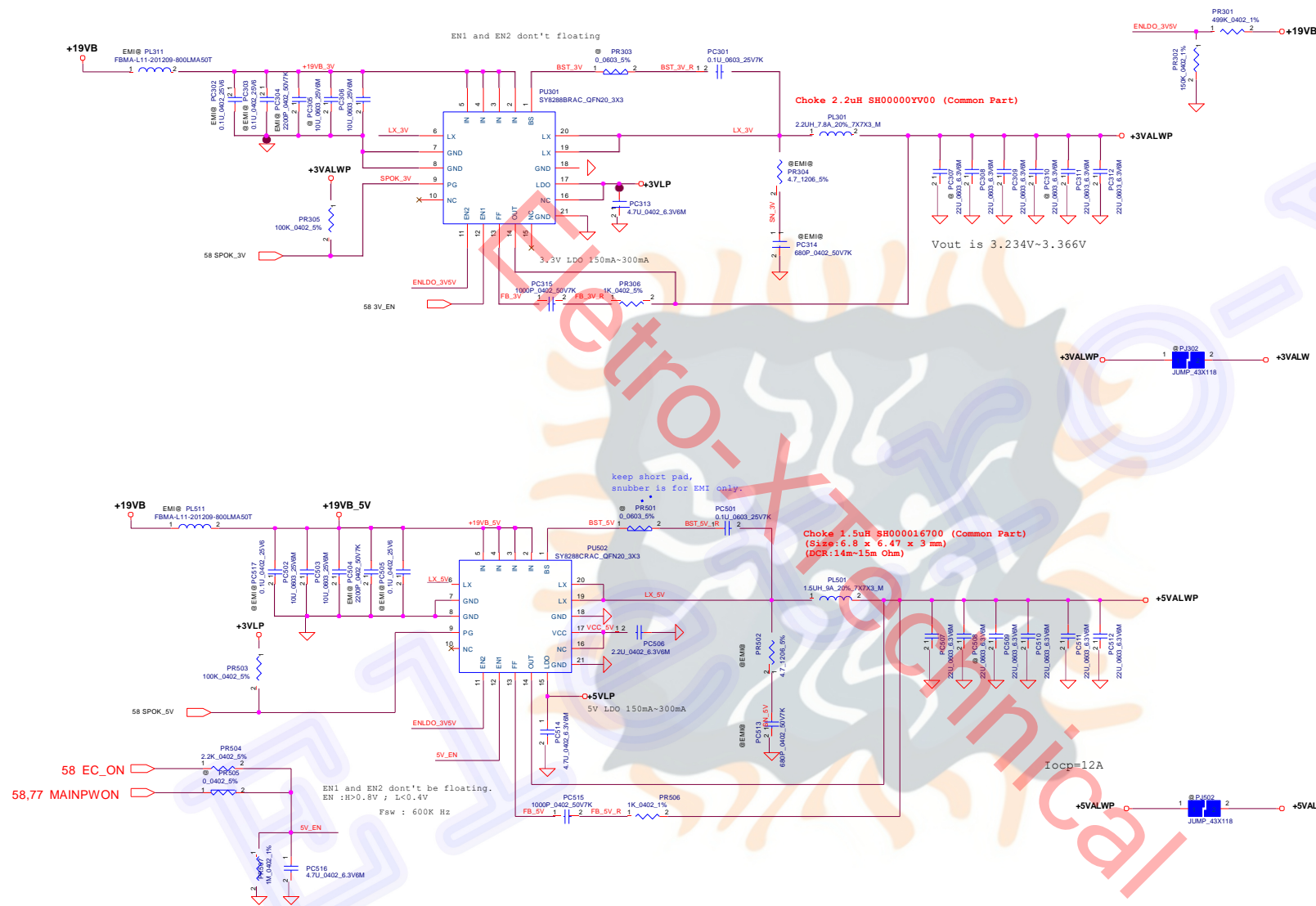
Reserve for 2-cell design

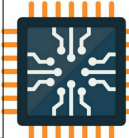
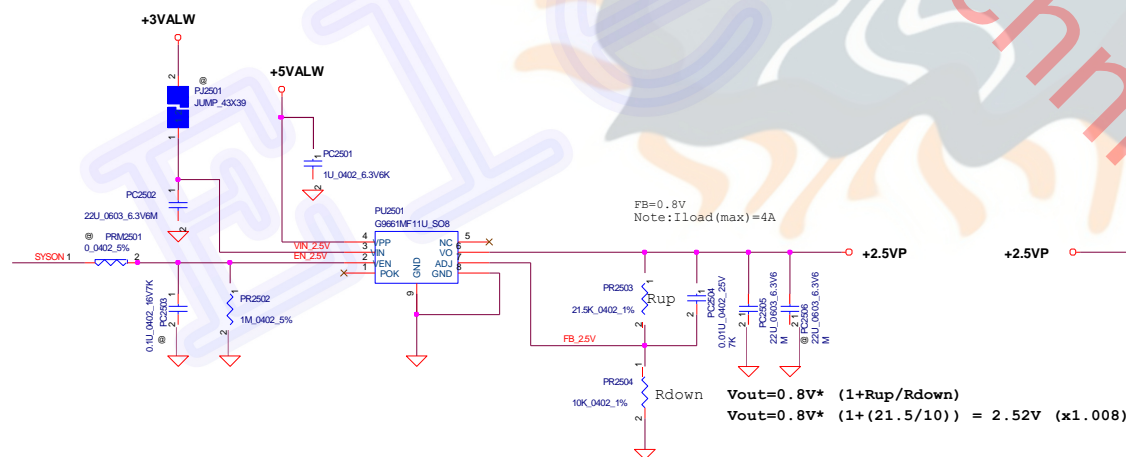
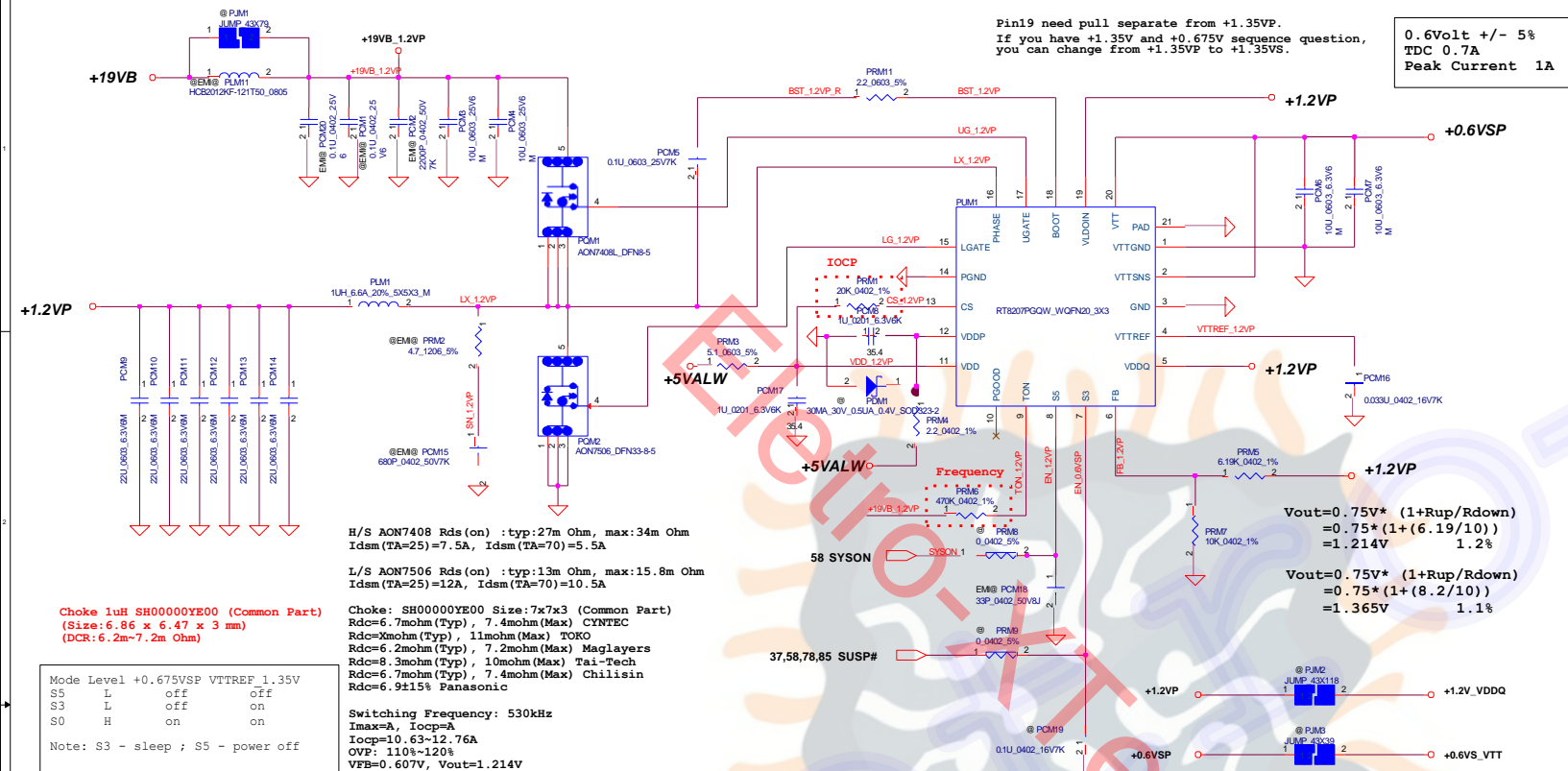




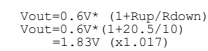
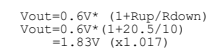
For 4S per cell 4.35V battery

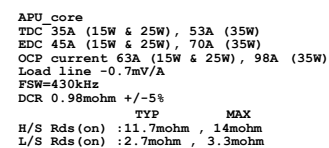


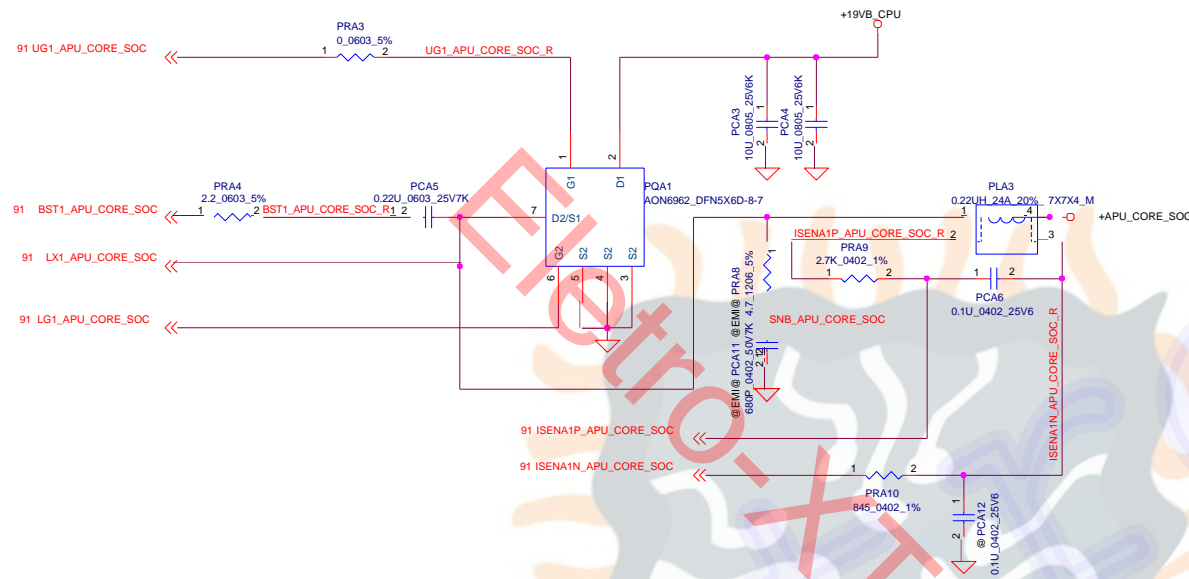




Time: 0.9VALW/1.8VALW



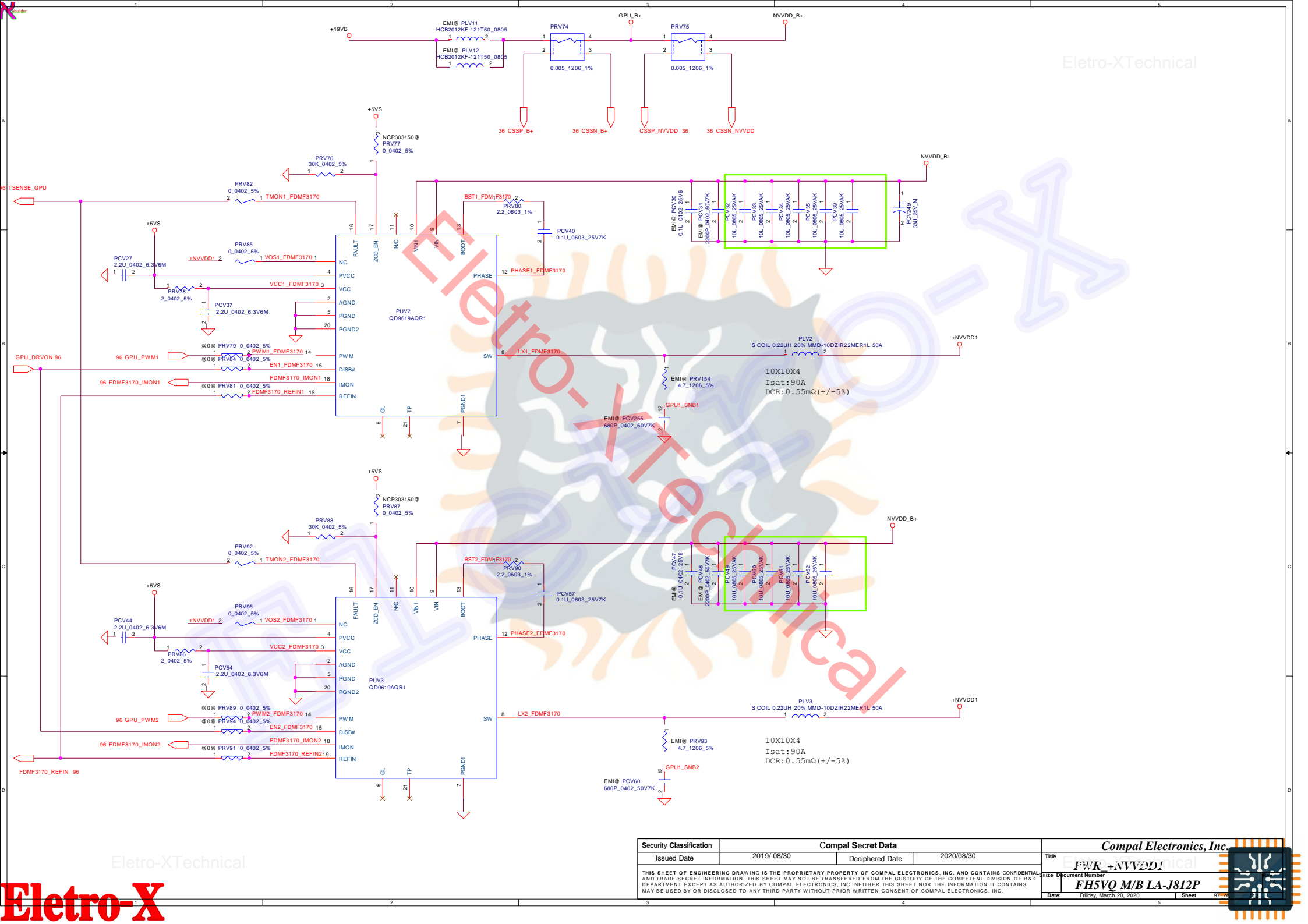




+APU_CORE_SOC

TDC 10A (15W & 25W & 35W)
EDC 13A (15W & 25W & 35W)
OCP current 24.2A (15W & 25W & 35W)
Load line -2.1mV/A
FSW=400KHz
DCR 0.98mohm +/-5%
TYP MAX
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

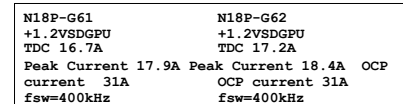
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/08/30	Deciphered Date	2020/08/30	Title	Reserve Page
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					FH5VQ M/B LA-J812P
				Date:	Friday, March 20, 2020
				Sheet	93 of



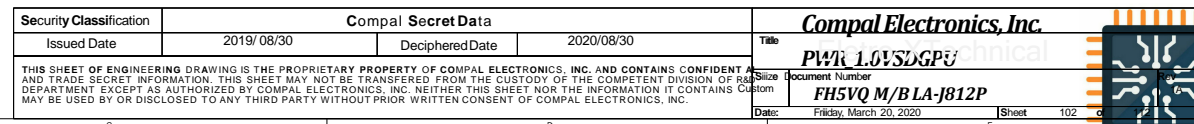
Eletro-XTechnical

Eletro-X

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/08/30	Deciphered Date	2020/08/30	Title	FWR +NVVDD1
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				FH5VQ M/B LA-J812P	
				Date:	Friday, March 20, 2020
				Sheet	97

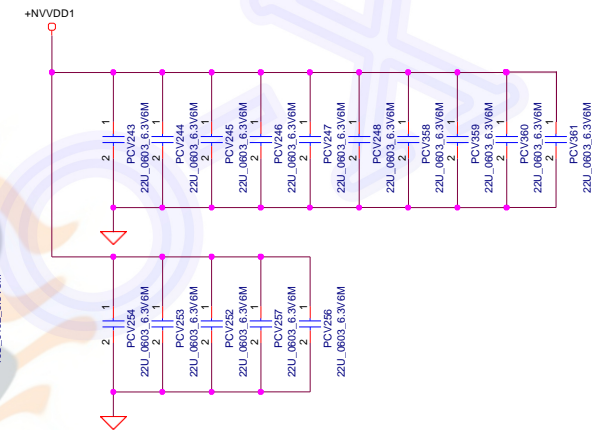
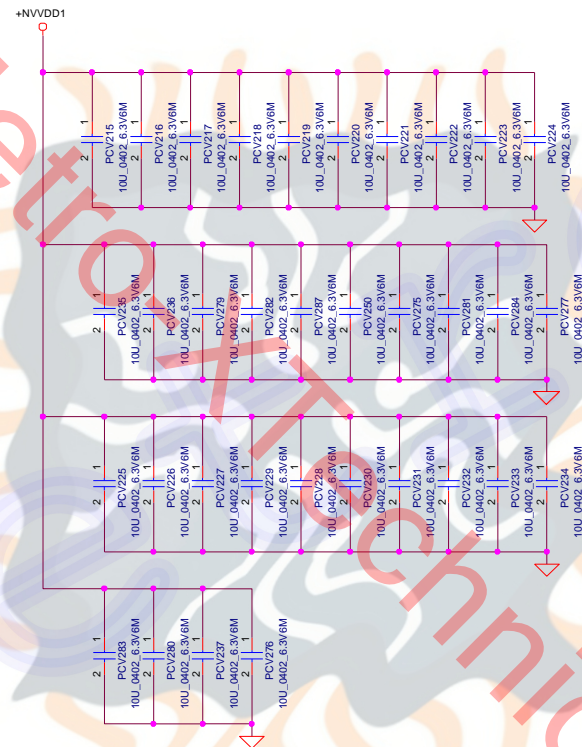
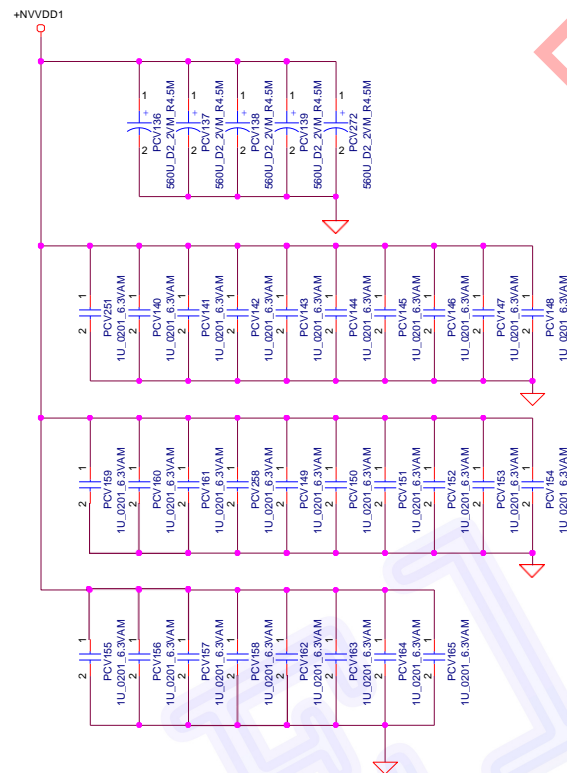


When, VRAM_VDD_CTL=Low
Vboot=1.2V

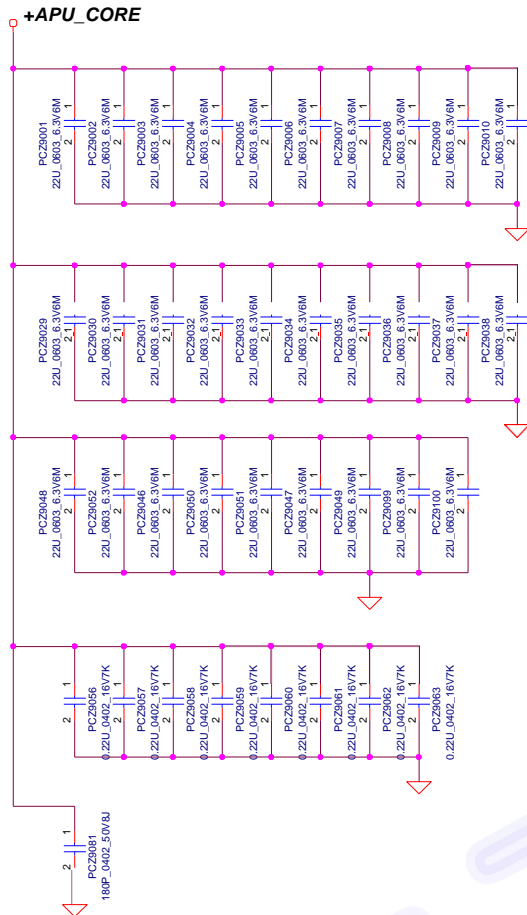


```
N18P-G0
+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28
```

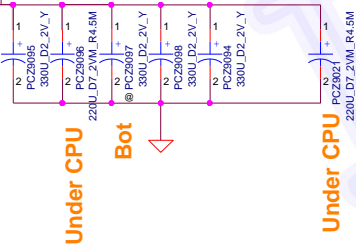
Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side) ¹		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)



+APU_CORE



+APU_CORE



Under CPU

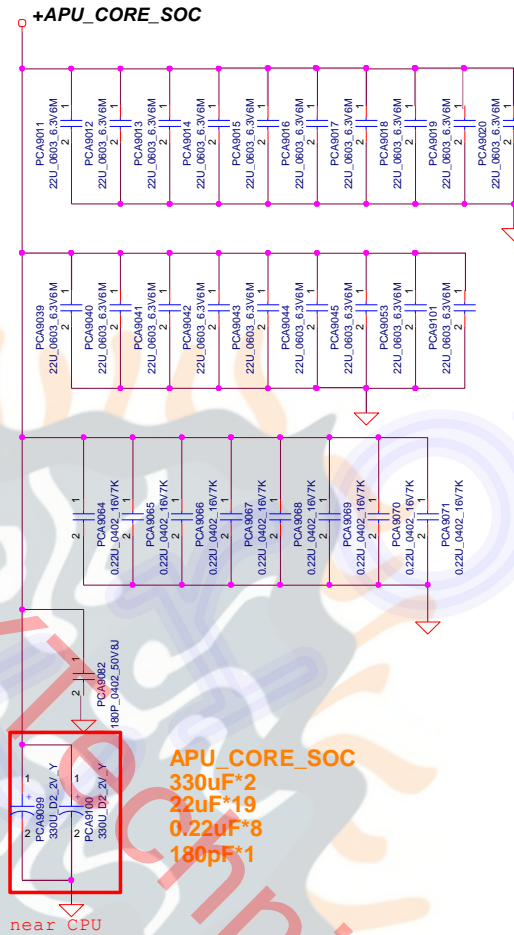
Bot

Under CPU

330u is common part SGA00009S00

APU_CORE
330uF*5
22uF*29
0.22uF*8
180pF*1

+APU_CORE_SOC



near CPU

330u is common part SGA00009S00

APU_CORE_SOC
330uF*2
22uF*19
0.22uF*8
180pF*1

Eletro-XTechnical

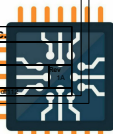
Eletro-XTechnical

Eletro-X

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/08/30	Deciphered Date	2020/08/30	Title	+APU_CORE Cap
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				Custom	FH5VQ M/BLA-J812P
				Date	Friday, March 20, 2020
				Sheet	95



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	update main source	0.1	88, 85	change PQM2 from EMB12N03V to AON7506 change PQM1 from EMB20N03V to AON7408L change PQB4 from 2N7002KW to L2N7002SWT1G	2019/11/20	A
02	prevent B2B mos damage	prevent B2B mos damage and reserve PDC function	0.1	85	pop PCB36, PRB37, PRB38 for PDC function	2019/12/24	A
03	ESD test improve	for ESD request	0.2	88	pop PCM18 33P_0402_50V&J for ESD request	2020/1/2	B
04	change 0ohm to R-short	deduce 0ohm part count	0.2	85, 96, 97, 100, 102	change PRV84, PRV20, PRV56, PR1010, PRB14, PRV91, PRB25, PRV79, PRV89, PRV81, PRW9, PRV94, PRB17, PRB22, PRV145, PRW20, PRV146, PRV34, PRB33, PRV54 From 0ohm to R-short	2020/1/2	B
05							
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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	58	Others	12/11	BOM Option for DVT/PVT/MP	R1564 option for DVT/PVT/MP	DVT	1.0
2	06	Others	12/11	Add DVT PCB Information	Add ZZZ for DVT PCB	DVT	1.0
3	40	HDMI	12/13	Mask un-used co-lay HDMI component	Change L2513, L2514, L2515 symbol to INPAQ_HCM1012GH900BP_4P-npm Change R756, R765 symbol to R_0402-npm	DVT	1.0
4	10	Others	12/18	Mask un-used co-lay component	Change JC1 symbol to ACES_91960-0084N_8P-npm	DVT	1.0
5	27	GPU	12/25	Crystal frequency adjust	CV1, CV2 change to 15pF	DVT	1.0
6	27	GPU	12/25	Update GPU PN	UV1 PN change for PS sample (SA0000CZO30/SA0000CZP30)	DVT	1.0
7	52 09	Others	12/25	Un-pop un-use wake/I2S/UART interface	Un-pop RM114, RM115, RM145, RM146, RM141, RM142, RM143, QM1 Un-pop RC757, RC758, RC759, RC760	DVT	1.0
8	68	MSATA	12/25	Update component BOM structure for MSATA	RM138 with MSATA@	DVT	1.0
9	27	GPU	12/25	Update BOM structure for non-GC6	Pop RV414 RV415 with @	DVT	1.0
10	11	RTC	12/28	Update for RTC Power Consumption	Pop UC8 Un-pop UC67, RC6184, RC6185	DVT	1.0
11		Others	01/02	Change 0 ohm to R-Short	0603 package --> R41 0402 package --> RS137, RS148	PVT	1A
12	27	GPU	01/06	UV51 PN change	UV51 PN change from SA0000D6900 to SA0000DH100	PVT	1A
13	63	TP	01/16	Add Capacitor for ESD require	Add C2762	PVT	1A
14	27	GPU	01/20	Update GPU PN for G61-MP2	0	PVT	1A
15	58	Others	03/09	BOM Option for MP	R1564 option for MP	MP	1A

